Green wafers can lower costs and reduce carbon emissions in manufacturing

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Abstract

While solar photovoltaics (PV) produce no greenhouse gas (GHG) emissions during operation, significant GHG emissions are associated with their production and transportation.
As the world transitions to renewable energy sources and moves to a hydrogen economy, PV have to become greener. Silicon wafers are the most energy-intensive component of a PV module. Conventional wafer production contains several high-temperature processes, such as polysilicon production and ingot pulling. NexWafe offers a cleaner, more efficient and cheaper solution. Our EpiNex™ wafers enable higher efficiencies, lower costs and reduced carbon emissions in wafer manufacturing by more than 70% when compared with the conventional Czochralski process in regions that rely on coal-based electricity. NexWafe's innovative and unique technology creates the opportunity to profitably manufacture ultra-low-carbon green solar wafers.

Introduction

The energy transition and the move towards a green hydrogen economy are motivated by the need to limit global warming. The Intergovernmental Panel on Climate Change (IPCC) has shown that global warming can be stopped if the deployment of renewable energies is accelerated. However, the window of opportunity to achieve the 1.5°C Paris Agreement goal is closing fast.

In its 2021 *World Energy Transitions Outlook*, the International Renewable Energy Agency (IRENA) envisions that solar PV capacity will need to reach more than 14,000 GWp cumulatively by 2050 [1] for the energy transition to be reached. At the same time, the estimated remaining carbon budget from the beginning of 2020 to limit global warming to 1.5°C with a likelihood of 83% is less than 300 Gt CO_2 [2].

This puts a limit on how much CO_2 can be emitted, even while producing renewable energy infrastructure, such as photovoltaic (PV) modules.

Crystalline-silicon-based PV is the dominant technology for the deployment of solar energy today. Impressive cost reductions in silicon-based PV have been achieved by scaling up production over the past two decades. However, the need remains for increased efficiencies, further lowering production costs and reducing the greenhouse gas (GHG) emissions associated with the production of PV modules.

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Results from modelling by Müller et al. show the potential environmental impacts: solar modules produced in China are linked to emissions of 810 kg CO_2-eq/kWp of which 62.7% can be directly attributed to wafer production [3].

To put this into perspective, producing the required 14,000 GWp of PV modules with conventional technology alone would consume more than 3% of the world's remaining CO_2 budget. In light of this, it is imperative for PV manufacturing to become greener and more efficient.

NexWafe's direct gas-to-wafer technology offers a pathway to reduce the carbon emissions in wafer production by more than 70%, cutting the emissions of module production by half.

Conventional wafer production

Wafers are produced in an energy-intensive process chain. Conventional wafer production is inherently complex and involves the following main energy-intensive and resource-inefficient steps: polysilicon production, crushing, ingot pulling, cropping, squaring, bricking and sawing.

Polycrystalline silicon is the key feedstock in the crystalline-silicon-based PV industry. The so-called Siemens process is the most widespread for the production of polysilicon. In a Siemens reactor, graphite electrodes pass current through a U-shaped silicon core. Trichlorosilane (TCS) and hydrogen are injected into the reactor. At the hot silicon surface, the TCS undergoes hydrogen reduction in a process similar to chemical vapour deposition (CVD) to form solid silicon and gaseous hydrochloric acid. Solid polysilicon deposits onto the silicon seed. After the process is complete, the large rods are broken into chunks or chips of various sizes.

Monocrystalline ingots are typically manufactured via the Czochralski (Cz) process. Polysilicon is melted in a quartz crucible. A seed

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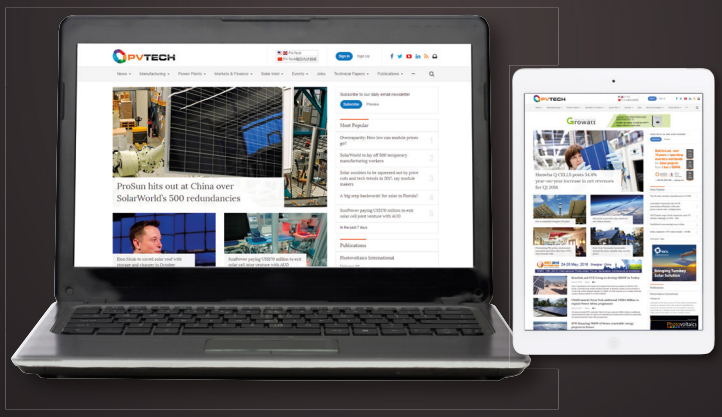

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crystal is dipped into the melt and pulled slowly upwards while being rotated. Since crystal growth occurs at the melt/ingot interface, a cylindrical single-crystal ingot is produced. The silicon grown via the Cz process is characterised by a relatively high oxygen concentration. Another disadvantage of the Cz process is the fact that the dopant distribution is not uniform along the ingot because the segregation coefficient of dopants such as gallium or phosphorus is not unity. This results in a relatively low dopant concentration, hence higher resistivity, at the start of the Cz pulling process and a higher dopant concentration, hence lower resistivity, towards the end of the pulling process.

Following cooling of the finished ingot, its top and tails are removed, and the cylindrical ingot is squared to leave a square or pseudo-square ingot. The squared ingot is then cut into shorter bricks, which are finally sliced into wafers by a wire saw. Wire sawing is an inherently wasteful process due to the unavoidable losses of silicon. Even with today's extremely thin diamond-coated wires, about 30% of the silicon in the bricks is lost.

The EpiNex process – kerfless epitaxial growth of silicon wafers

Various kerfless wafer-manufacturing approaches have been developed to reduce the amount of silicon used. Such kerfless technologies include 1366's direct wafer technology [4], which produces multi-crystalline wafers from the liquid phase, and SiGen's PolyMax technology [5], which separates thin layers from a brick using hydrogen implantation. While some of these approaches have shown the potential to reduce costs, they also compromise the efficiency mainly due to the limitations in the quality of the wafers produced.

In the 1990s, the potential was recognised of epitaxial growth on restructured porous silicon substrates to offer lower manufacturing costs while maintaining or even enhancing solar efficiency. A good overview of the early work on layer-transfer processes for crystalline solar cells is given by Brendel [6]. Since then, several research groups such as ISFH and IMEC worked on improvements of this so-called porous silicon (PSI) process. In 2018, Gemmel et al. grew epitaxial wafers on polished seed wafers, with a resistivity of 3 Ωcm and an

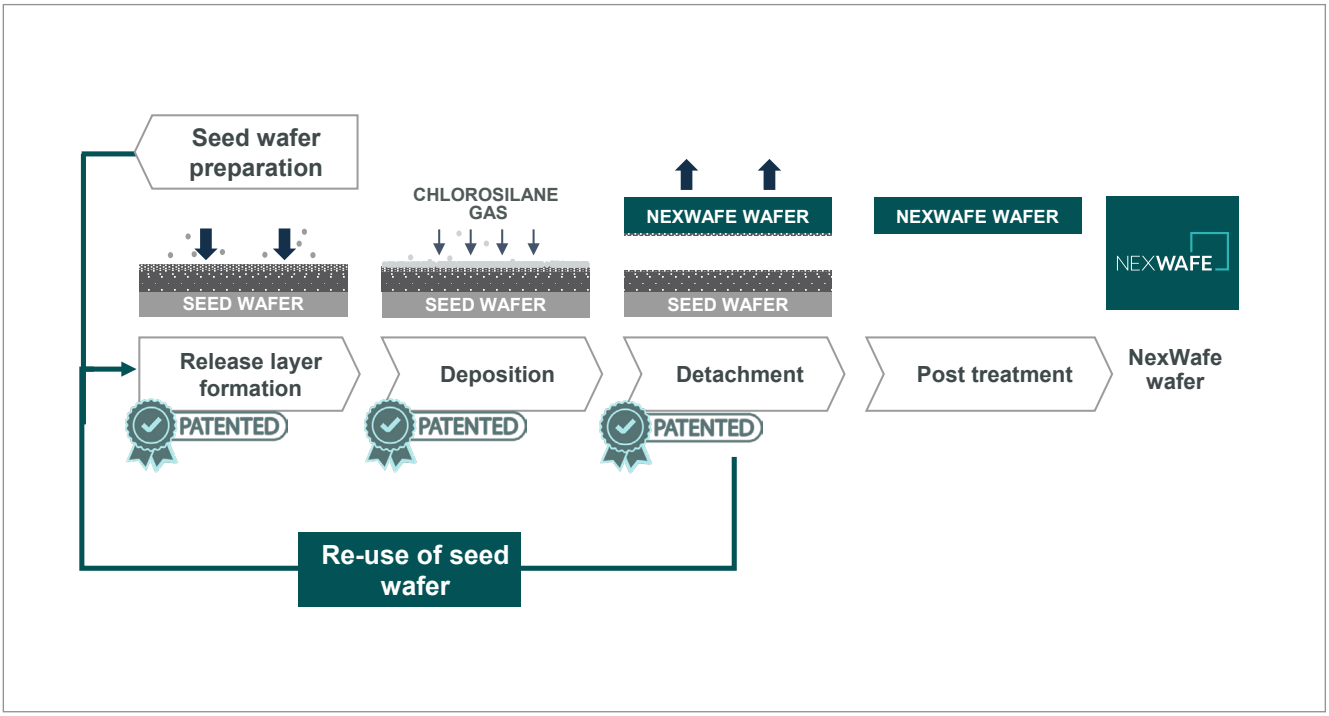


Figure 1: Direct gas-to-wafer process chain

average minority carrier lifetime (MCLT) of 3.2 ms, which could be improved by gettering to very high lifetimes of 4.6–8.0 ms [7]. Solexel and Crystal Solar tried to commercialise a PSI process. In cooperation with IMEC, Crystal Solar demonstrated high solar-cell efficiencies on epitaxially grown wafers but failed to scale-up its technology [8].

NexWafe's direct gas-to-wafer technology (Figure 1) to produce epitaxially grown (EpiNex) wafers is also based on the principles of the PSI process. Unlike earlier attempts, NexWafe's technology builds on processes and equipment that allow high throughput, low cost and large wafer sizes, as demanded by the PV industry.

In the first step, Cz wafers with a resistivity of 10 mΩcm are prepared for use as seed wafers. Chemical mechanical polishing steps, which are common in the semiconductor industry to create 'epi-ready' wafers, are prohibitive in the solar industry because of the associated high cost. Instead of using epi-ready wafers, NexWafe buys Cz wafers and cuts and etches them using a wet chemical etching tool. This tool was designed for solar-cell production to eliminate saw damage and create a surface suitable for the subsequent release layer formation and the epitaxial growth of high-quality EpiNex™ wafers.

Using a proprietary equipment design suitable for high throughput, anodic oxidation is used to create a few microns-thin porous silicon layers on one surface of the seed wafer. Good homogeneity of the porous layers across the total wafer surface is essential. At the same time, a stack of low porosity and high porosity layers is created to enable good detachability and high quality of the EpiNex™ wafer. Figure 2 shows a porous layer stack with a low porosity layer (LPL) at the surface and a high porosity layer (HPL) below the LPL.

Subsequently, the porosified seed wafers are transferred to the epitaxy reactor. During heating to the deposition temperature of over 1100°C, the porous structure reorganises. The pores at the surface of the LPL close and a monocrystalline layer is formed, which then acts as a template for the epitaxial growth. At the same time, the voids of the HPL grow and it transforms into a microscopic cathedral – a large, open space where the roof is supported by a few thin columns.

After reorganisation of the porous layers, the wafers are transferred into the deposition chamber. At temperatures of about 1100°C, silicon is grown by atmospheric pressure chemical vapour deposition (APCVD) from a mixture of chlorosilane and hydrogen. Phosphine or diborane can be used as dopants to grow either n-type or p-type wafers.

The epitaxially grown wafers are mechanically detached from the seed wafers. After the excess silicon, which has grown over the edges of the seed wafer, is removed by grinding or laser scribing, the sandwich consisting of the seed wafer and the EpiWafer is taken by a vacuum gripper and placed on a second vacuum chuck. After applying a vacuum to both sides of the sandwich, the EpiWafer is detached from the seed wafer by applying mechanical stress. The process has been integrated into a fully automated tool, which performs the wafer handling, positioning and detachment.

After detachment, both the seed wafer and the EpiWafer are chemically cleaned to remove the residues of the release layer. A phosphorus-diffusion for gettering, which is a well-known treatment to increase the effective lifetime by reducing extrinsic minority carrier recombination, is applied to the EpiWafer [9]. The seed wafer is reused.

EpiWafer properties

Oxygen content

Oxygen impurities in Cz silicon wafers arise from the dissolution of the quartz crucible used during ingot pulling. Boron-oxygen complexes cause light-induced degradation of solar cells. The PV industry has mitigated this problem by moving towards more expensive gallium-doped wafers. Oxygen creates various kinds of defects in silicon crystals, which can reduce MCLT and thereby reduce cell efficiency [10]. The EpiNex process produces EpiWafers with a lower oxygen concentration of more than an order of magnitude than that of Cz wafers (Figure 3).

NexWafe believes that the low oxygen content inherent to the EpiNex process can enable significant cell efficiency gains versus conventional Cz wafers.

Minority carrier lifetime

The MCLT of a wafer is an important aspect for the electronic quality of a wafer. The MCLT is determined by the quasi steady-state photoconductance (QSSPC) technique [11]. Conventional n-type Cz wafers for solar-cell production are specified to have an MCLT exceeding 1ms for resistivities of 1–7 Ωcm [12]. EpiWafers produced by the EpiNex process meet the industry standards (see Figure 4).

"...the EpiNex process can enable significant cell efficiency gains versus conventional Cz wafers."

Resistivity control

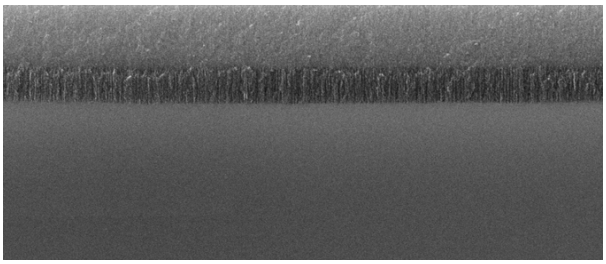
As discussed in Section 2, doping levels and therefore resistivity vary from one end of an ingot to the other. The resistivity can be seven times lower at the top end than the tail end for n-type ingots [13]. Wafers from the top of the ingot exhibit low doping, high resistivity and high MCLT. Cells fabricated from such wafers exhibit relatively high open-circuit voltage (VOC) but low fill factor (FF). Wafers from the bottom of the ingot provide high doping, low resistivity and low MCLT, and typically exhibit a lower VOC but higher FF. In addition, the longer the crucible is used, the more impurities tend to accumulate in the melt, which will result in a lower MCLT and lower cell efficiencies.

In contrast, the EpiNex process produces wafers doped by adding dopants to the gas phase. The doping level can thus be controlled very accurately by mass flow controllers. As a result, EpiWafers exhibit a very narrow resistivity distribution (Figure 5).

A narrow resistivity distribution allows all wafers to be processed in as close to optimal conditions as possible. Increased average cell efficiency from the cell-manufacturing line and a narrow distribution of cell efficiencies can be achieved.

As discussed, the doping gradient along the length of a Cz ingot is a problem, but the creation of doping gradients within a wafer (i.e. from the surfaces of the wafer to the bulk of the wafer) can be an advantage. Such doping gradients could result in reducing the recombination of carriers in the bulk while maintaining good contact properties. Doping gradients within the wafer could also increase cell efficiency. However, such gradients cannot be produced in conventional wafer manufacturing, but they can be created during the EpiNex manufacturing process simply by changing the dopant concentration during the deposition process. Doping from the gas phase allows a high level of control of the doping level.

a)



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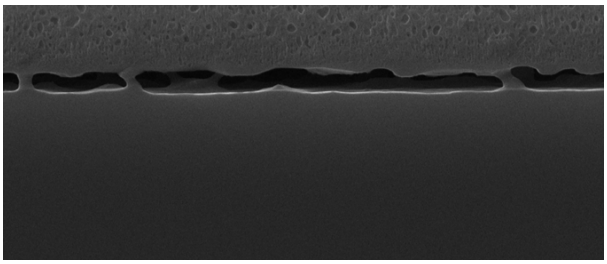

Figure 2: Porous silicon stack (a) after anodic oxidation and (b) after reorganisation

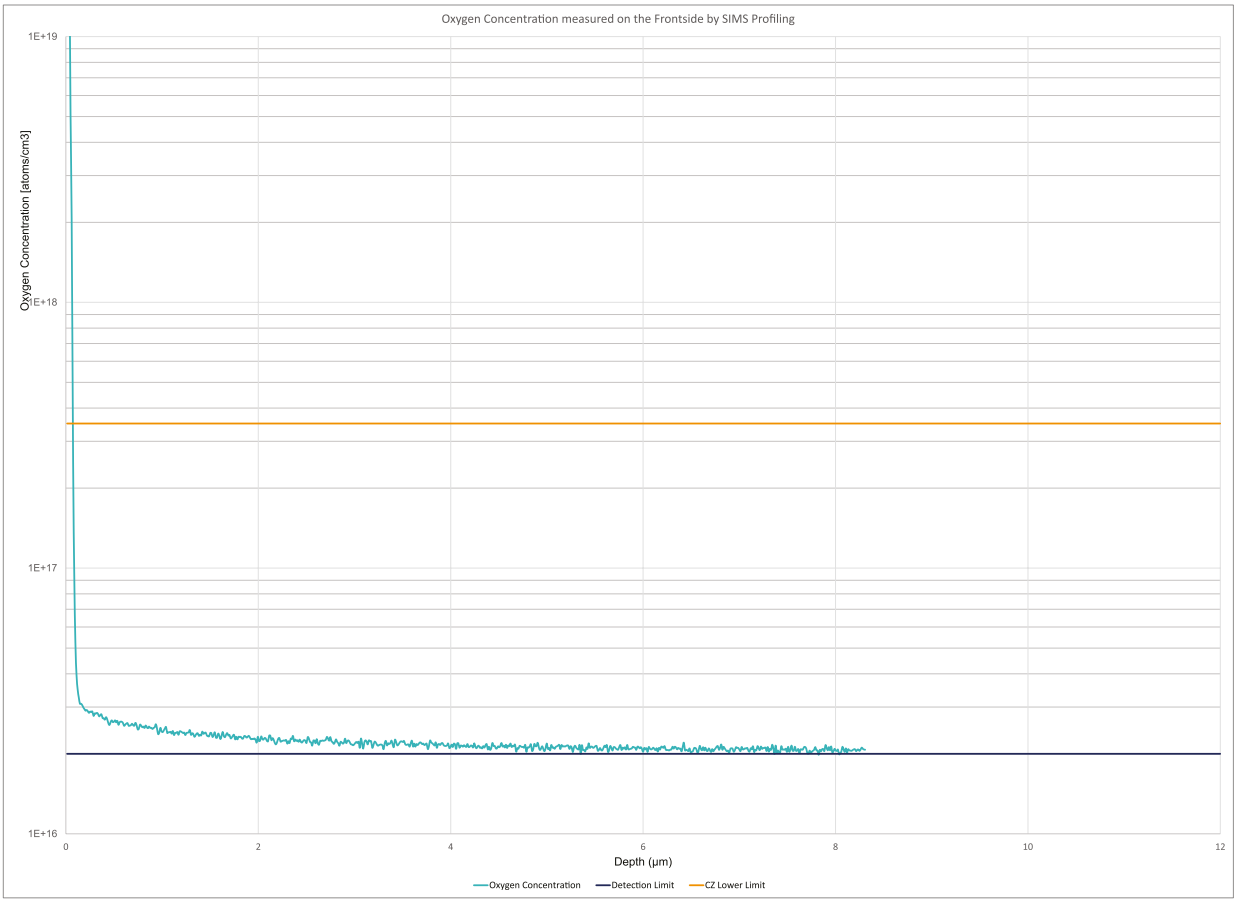

Figure 3: Oxygen concentrations of EpiWafer and Cz wafers

Wafer size

During recent years, PV-wafer manufacturing has been moving towards larger wafer formats. The previously dominant M2 has been replaced by larger formats such as M6 (pseudo-square, 166 mm side length), which are now being phased out as the major PV companies move towards the larger M10 (pseudo-square, 182 mm side length) and G12 (full-square, 210 mm side length) wafer formats. As wafer size increases, the risk of lower manufacturing yields also increases. Yield rates are reported to be lower for G12 in the wafering process, which is an issue that may be amplified by any transition towards thinner wafers or even larger wafer formats. At the ingot level, pull speeds for G12 ingots are reportedly around 20–25% slower than for M6 or M10 ingots, resulting in increased costs. In addition, the G12 format is full-square. Large wings are cut off in the squaring process, which can be recycled but they reduce the energy efficiency of the manufacturing.

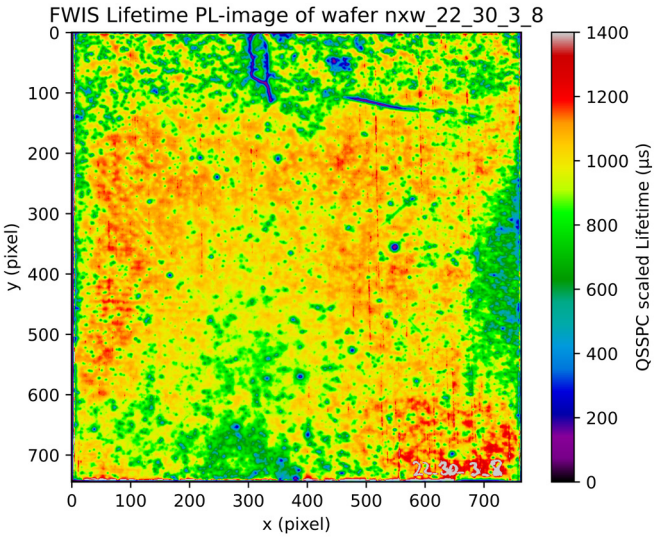

Figure 4: Photoluminescence measurement of an EpiWafer with 1 Ωcm resistivity

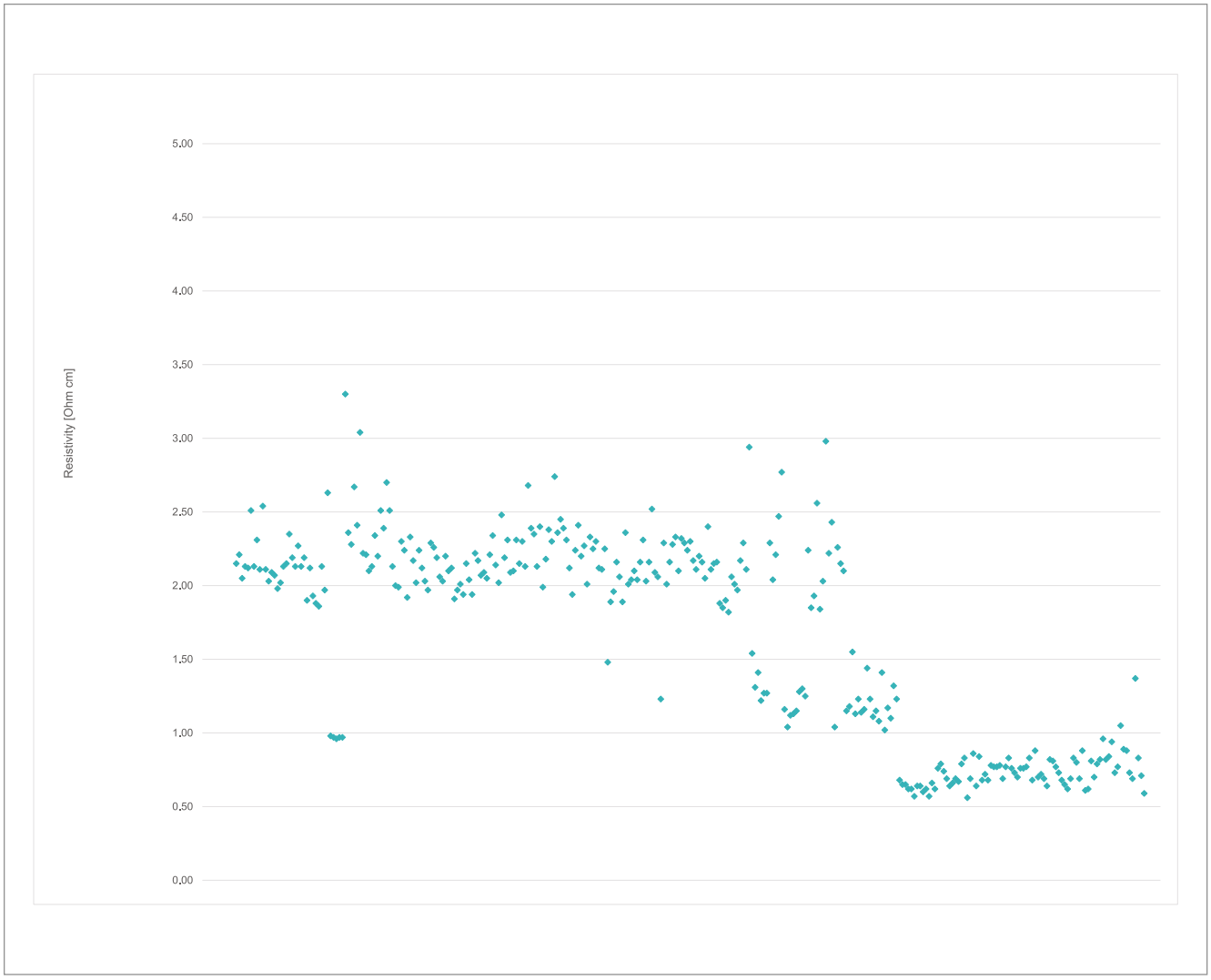

Figure 5: Resistivity of wafers grown by the EpiNex process

An advantage of the EpiNex process is its inherent flexibility regarding changes in wafer formats. It can cope with any wafer size as long as seed wafers of the same size are available and fit on the carrier system, which has an area of approximately 1 m2. The EpiNex process is fully compatible with all current wafer formats, but it is not exposed to the challenges of G12 manufacturing such as reduced ingot pull speed or lower energy efficiency.

Wafer thickness

NexWafe's EpiNex process offers an opportunity to produce the thin wafers that modern cell processes require, and the company has already demonstrated the production of wafers with a thickness of approximately 50 µm (see Figure 6).

The optimal wafer thickness depends on various factors, including the quality of the surface passivation and the quality of the wafer. For HJT cells, for example, the very good passivation at both the front and rear surfaces means that the optimum wafer thickness is below 100 µm. At PV CellTech 2022, Risen Energy calculated an efficiency gain of about 1% absolute for HJT cells by reducing the wafer thickness from 150 µm to 80 µm.

The ITRPV roadmap 2022 [15] predicts that the wafer thickness of conventionally produced wafers will drop to 125 µm but only over the course of 10 years, and further decreases are unlikely to be achievable for conventional wafer production at an acceptable throughput and yield.

While the use of thin wafers below 120 µm thickness requires advances in PV-cell manufacturing, in particular improvements in certain handling steps, 90–100 µm-thick wafers should be viable in cell and module manufacturing by 2026. The development will be driven by the need to unlock the true potential of high-efficiency cell architectures.

Carbon footprint

As discussed above, conventional wafer manufacturing has many inherently energy-intensive process steps and there is also high

silicon waste due to kerf loss. The EpiNex process – a direct gas-to-wafer process – offers significant energy and carbon savings. In a comprehensive life-cycle assessment in 2020, Fraunhofer ISE compared the carbon footprint of EpiWafers with that of wafers manufactured using conventional manufacturing processes (polysilicon production by the Siemens process, Cz ingot pulling and diamond-wire wafer sawing). However, it must be noted that a like-for-like comparison should also take into account that EpiWafers have no saw damage. Thus, an EpiWafer with a 15–20 µm lower thickness than an as-cut Cz wafer gives the same solar cell thickness. Fraunhofer found that the EpiNex process offers significant potential for carbon footprint reductions (see Figure 7). The exact amount of the CO_2 footprint reduction is dependent on the site selected for manufacturing and the wafer thickness. Taking into account the compatibility of EpiWafers with very low wafer thicknesses, CO_2 footprint reductions of up to 70–75% were found to be possible. Even when comparing like-for-like in both manufacturing location and wafer thickness, the data from the study implies that CO_2 reductions of approximately 50% could be achieved.

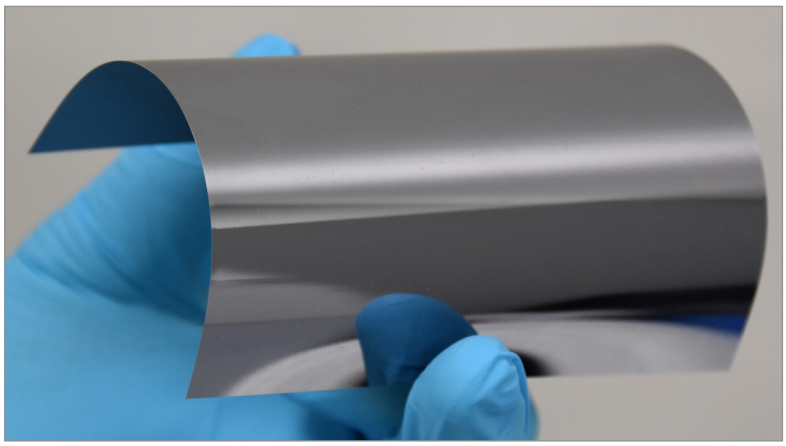

Figure 6: EpiWafer with 51 µm thickness

The increasing awareness of buyers and governments of the environmental impact and CO_2 payback time of PV modules will drive the industry to reduce its CO_2 footprint. Since almost 63% of the GHG emissions in module manufacturing stem from wafer production, the EpiNex process appears to be a clear opportunity

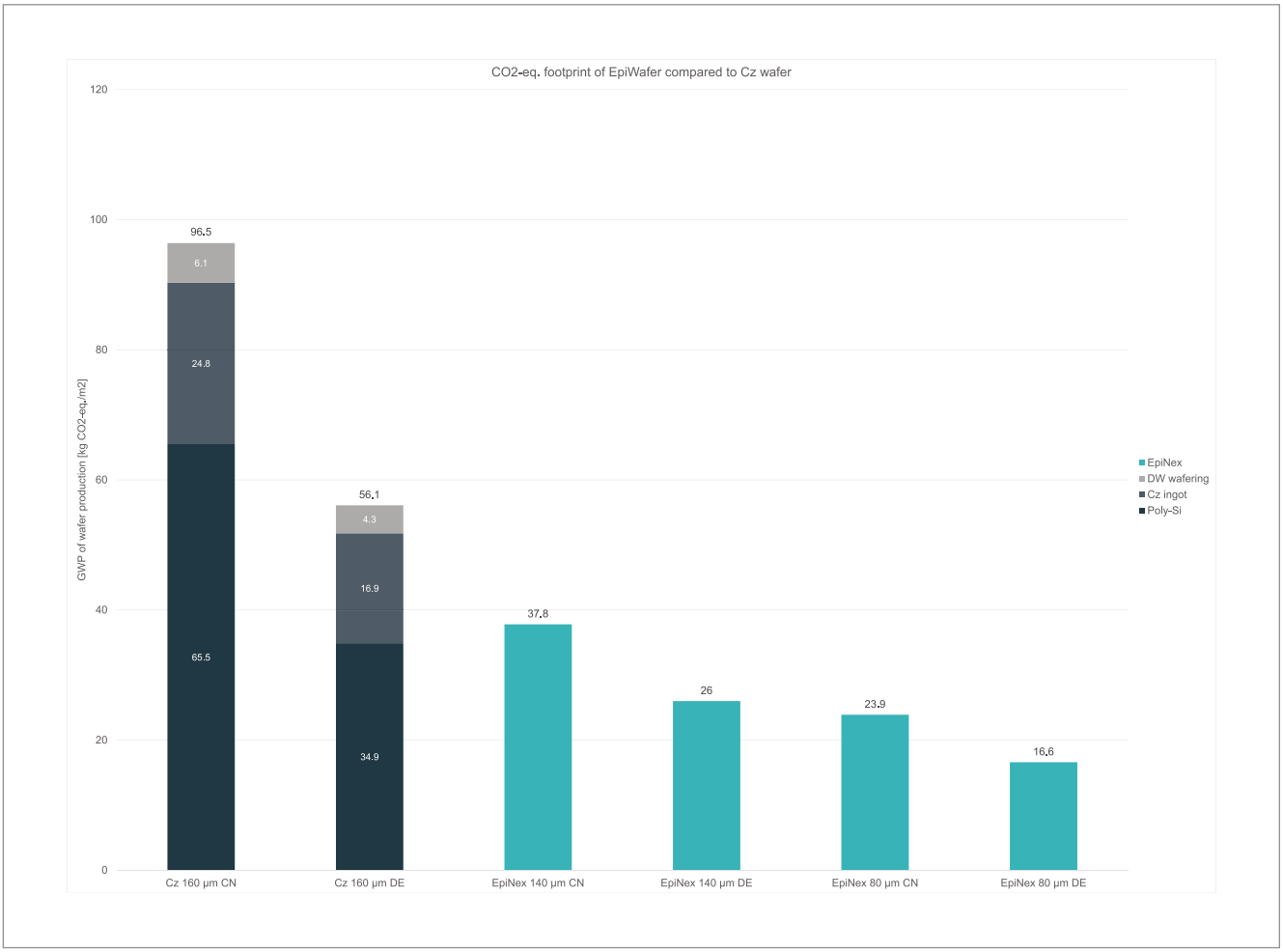

Figure 7: CO_2-equivalent footprints of the EpiWafer process versus conventional wafer manufacturing. CN refers to manufacturing in China; DE refers to manufacturing in Germany.

Source: Fraunhofer ISE

to reduce the GHG emissions of PV-module manufacturing by 30–50%. Using green solar EpiWafers would allow PV-module manufacturers to differentiate their offering from the competition and would help to accelerate the global reduction of GHG emissions.

Summary and outlook

Accounting for 60% of renewable capacity additions in 2021 [14], solar PV is moving fast towards becoming the single most important source of a sustainable global energy system. Nonetheless, expert projections are painfully clear in assessing that the current trajectory of the energy transition is nowhere near the Paris Accord's 1.5°C pathway. Reaching the required 5200 GW of installed solar PV capacity by 2030 – a seven-fold increase compared with 2020 levels – and over 14,000 GWp by 2050 for a net-zero scenario is a massive undertaking. But a mere focus on increasing installed capacity is not enough.

Current solar PV wafer-manufacturing techniques are costly and inefficient, with a significant carbon footprint. This is particularly true for the production of the most expensive and energy-intensive part of a module: the solar wafer.

Applying proven methods from electronics in its EpiNex process, NexWafe has set out to change that with a clear goal in mind: producing green solar wafers at scale for half of their current cost, with dramatically lower CO_2 emissions and superior quality.

The results derived from NexWafe's prototype production are very promising: oxygen impurity levels are an order of magnitude lower than those of Cz wafers, the EpiNex process has shown to be compatible with all current and upcoming wafer sizes – from M2 to G12 – and wafer thicknesses of down to approximately 50 µm have been reached. Also, the associated CO_2 emissions of EpiWafer production have been up to 70–75% lower than for Cz wafers, translating to a reduction in carbon emissions of 30–50% at a module level.

While it is clear that different manufacturing methods will coexist for the foreseeable future, NexWafe has many reasons to believe that its EpiWafers will be a highly competitive product that can help the PV industry to become greener and contribute to further reducing solar PV's levelised cost of electricity.

Backed by prominent industrial investors, NexWafe is planning to begin construction in 2023 on a 250 MW pilot production facility to demonstrate the commercial and technical specifications needed to meet customer requirements. With strategic partners, NexWafe will then be ready to move production towards the gigawatt scale.

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