Photovoltaics International

THE TECHNOLOGY RESOURCE FOR PV PROFESSIONALS

Edition 49

Perovskite tandem cells
Options for upscaling

High-efficiency POLO IBC cells
Based on PERC+ processing technology

TOPCon and shingle heterojunction cells
Edge passivation

Heterojunction technology
Status of development in China

Green wafers
Lowering costs and CO_2 emissions

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Foreword

Welcome to Photovoltaics International 49. As we reach the end of the first quarter of 2023, the PV industry continues to traverse a period of uncertainty, albeit punctuated by excitement and anticipation.

This is the first year in some time for the industry to witness signs of a very welcome renaissance in manufacturing across a number of locations around the world, with India, the US and Europe (most notably Turkey) currently in the process of placing purchase orders for new c-Si cell lines for fabs either planned or already under construction.

On the technology side, we are seeing TOPCon, heterojunction and other developing technologies continue to jostle for position as the long-term successor to PERC and in this edition we look at the current state of play in several areas.

Chinese manufacturers DAS Solar and Huasun have both contributed papers, the former discussing edge passivation of TOPCon and shingle heterojunction cells, with the latter focusing on the status of heterojunction technology in China.

Fraunhofer ISE has authored a paper discussing options for upscaling perovskite tandem cells, while ISFH's article looks at high-efficiency POLO IBC cells.

Finally, CEA-INES has written on the performance limits of shingle heterojunction modules and NexWafe on how green wafers can lower manufacturing costs and carbon emissions.

As always, our sincere thanks go to all our contributors and we hope you enjoy reading the journal.

Andre Lamberti
Editor-in-Chief
Solar Media

Editorial Advisory Board

Photovoltaics International's primary focus is on assessing existing and new technologies for "real-world" supply chain solutions. The aim is to help engineers, managers and investors to understand the potential of equipment, materials, processes and services that can help the PV industry achieve grid parity. The Photovoltaics International advisory board has been selected to help guide the editorial direction of the technical journal so that it remains relevant to manufacturers and utility-grade installers of photovoltaic technology. The advisory board is made up of leading personnel currently working first-hand in the PV industry.

Our editorial advisory board is made up of senior engineers from PV manufacturers worldwide. Meet some of our board members below:

Prof Armin Aberle, CEO, Solar Energy Research Institute of Singapore (SERIS), National University of Singapore (NUS)

Prof Aberle's research focus is on photovoltaic materials, devices and modules. In the 1990s he established the Silicon Photovoltaics Department at the Institute for Solar Energy Research (ISFH) in Hamelin, Germany. He then worked for 10 years in Sydney, Australia as a professor of photovoltaics at the University of New South Wales (UNSW). In 2008 he joined NUS to establish SERIS (as Deputy CEO), with particular responsibility for the creation of a Silicon PV Department.

Dr. Markus Fischer, Director R&D Processes, Hanwha Q Cells

Dr. Fischer has more than 15 years' experience in the semiconductor and crystalline silicon photovoltaic industry. He joined Q Cells in 2007 after working in different engineering and management positions with Siemens, Infineon, Philips, and NXP. As Director R&D Processes he is responsible for the process and production equipment development of current and future c-Si solar cell concepts. Dr. Fischer received his Ph.D. in Electrical Engineering in 1997 from the University of Stuttgart. Since 2010 he has been a co-chairman of the SEMI International Technology Roadmap for Photovoltaic.

Dr. Thorsten Dullweber, Head of PV Department at the Institute for Solar Energy Research Hamelin (ISFH)

Dr. Thorsten Dullweber is leading the PV Department and the R&D Group Industrial Solar Cells at ISFH. His research work focuses on high efficiency industrial-type PERC and bifacial PERC+ silicon solar cells, where he co-authored more than 100 Journal and Conference publications. Before joining ISFH in 2009, Thorsten worked as project leader for DRAM memory chips at Infineon Technologies AG. He received his Ph. D. degree in 2002 for research on $Cu(In,Ga)Se_2$ thin film solar cells. Thorsten is member of the Scientific Committees of the EU-PVSEC and SNEC conferences.

Dr. Wei Shan, Chief Scientist, JA Solar

Dr. Wei Shan has been with JA Solar since 2008 and is currently the Chief Scientist and head of R&D. With more than 30 years' experience in R&D in a wider variety of semiconductor material systems and devices, he has published over 150 peer-reviewed journal articles and prestigious conference papers, as well as six book chapters.

Florian Clement, Head of Group, MWT solar cells/printing technology, Fraunhofer ISE

Dr. Clement received his Ph.D in 2009 from the University of Freiburg. He studied physics at the Ludwigs-Maximilian-University of Munich and the University of Freiburg and obtained his diploma degree in 2005. His research is focused on the development, analysis and characterization of highly efficient, industrially feasible MWT solar cells with rear side passivation, so called HIP-MWT devices, and on new printing technologies for silicon solar cell processing.

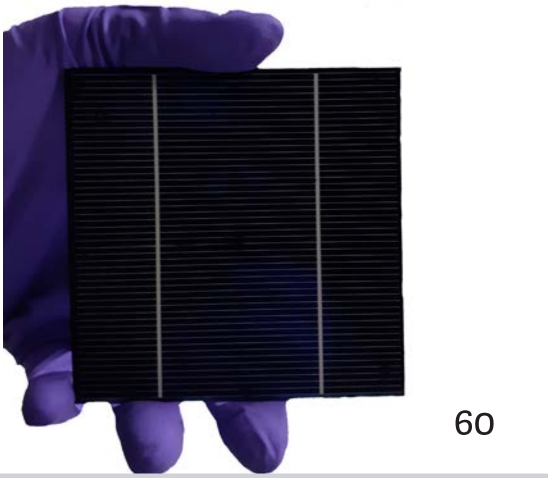
Dr. Jochen Rentsch, Head of department "Production technology – Surfaces and Interfaces", Fraunhofer Institute for Solar Energy Systems (ISE), Germany

Dr. Rentsch received his Ph.D degree in physics in 2005 from the Albert-Ludwigs University of Freiburg, Germany. He studied physics at the Technical University of Braunschweig and the University of Sussey (Brighton, UK) and obtained his diploma degree in 2002.
His current work focusses on the acquisition and management of public and industrial funded projects, the publication and licensing of R&D results, the transfer of processes and cell structures in the PV industry as well as consultancy on and auditing of PV manufacturing facilities worldwide.

Finlay Colville, Head of Market Intelligence, Solar Media

Finlay Colville joined Solar Media in June 2015 as head of its new Solar Intelligence activities. Until October 2014, he was vice president and head of solar at NPD Solarbuzz. Widely recognised as a leading authority on the solar PV industry, he has presented at almost every solar conference and event worldwide, and has authored hundreds of technical blogs and articles in the past few years. He holds a BSc in Physics and a PhD in nonlinear photonics.

Photovoltaics International remains the solar PV industry's only independent technical journal, carrying papers written by recognised industry experts and leaders in their field, highlighting technological innovation and manufacturing excellence to drive the sector forward. The PVI advisory board therefore plays a critical role in ensuring that the themes and topics covered in each volume of the journal are truly representative. Members of PVI publisher Solar Media's publishing team liaise with the advisory board on a regular basis and ahead of each volume of the journal to establish industry trends, qualify the journal's selection of papers and guarantee technical relevance. For more information on the Photovoltaics International advisory board, contact info@pv-tech.org.



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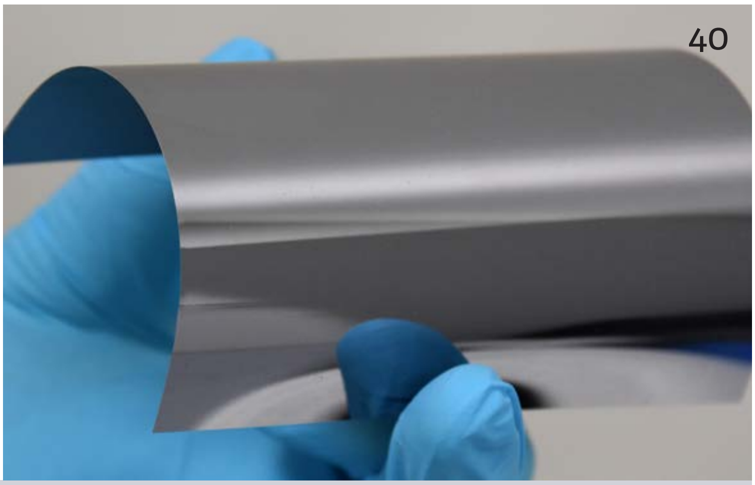

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News

US probe accuses Chinese solar manufacturers of evading tariffs
The US Department of Commerce has found that imports of some PV cells and modules produced in four Southeast Asian countries are circumventing antidumping duty and countervailing duty (AD/CVD) orders on solar cells and modules from China. In its much-anticipated preliminary determination published in December, Commerce found that solar companies are attempting to bypass US duties by doing minor processing in Cambodia, Thailand, Malaysia and Vietnam before shipping products to the US. The preliminary investigation into eight companies concluded that four – BYD Hong Kong (Cambodia), Canadian Solar (Thailand), Trina Solar (Thailand) and Vina Solar (Vietnam) – are circumventing duties, meaning their US imports may be subject to additional duties.
In addition, 22 companies were found to be non-compliant and will be subject to the most severe findings under 'adverse facts available'. These are mostly smaller companies, but the list includes the operations of LONGi subsidiary Vina in Malaysia, VSUN and contract manufacturer Flextronics in Malaysia, said supply traceability firm Clean Energy Associates in a briefing. Commerce's final determination is scheduled for 1 May 2023.

CAPACITY EXPANSIONS

LONGi to invest US$6.7 billion in building new production base in China
Solar manufacturer LONGi Green Energy Technology has announced an RMB45.2 billion (US$6.7 billion) plan to build a production base in China capable of manufacturing 100GW of solar wafers and 50GW of solar cells each year. In a filing to the Shanghai Stock Exchange, LONGi said it had signed a letter of intent with two local governments in the Shaanxi Province. The new base, which LONGi said will become the world's largest solar manufacturing facility, is expected to begin operations in the third quarter of 2024. The company's capacity expansion instantly attracted industry attention and speculation. Its chosen location for the installation is not necessarily the best choice for such a large-scale facility. After all, Inner Mongolia, Yunnan and other regions with relatively cheap electricity prices are arguably more attractive for large manufacturing sites.

JA Solar to build US$5.9 billion PV industry hub in China
Chinese module manufacturer JA Solar will invest RMB40 billion (US$5.9 billion) to construct a vertically integrated PV industry hub in Inner Mongolia, China. According to a filing published on 19 January, JA Solar had signed an agreement with the government of Ordos, one of the twelve major subdivisions of Inner Mongolia, to produce 100,000 tons of photovoltaic raw materials, 20GW of solar wafer capacity, 30GW of cells and a 10GW PV module plant. However, the filing did not disclose more details about the hub and the construction schedule.

Tongwei maintains PV module manufacturing push with plans for new 25GW factory
Polysilicon supplier Tongwei continues to expand its solar footprint, revealing plans in December to set up a 25GW module manufacturing base in the Nantong Economic and Technological Development Zone, in China's Jiangsu province. Expected to require an investment of around RMB4 billion (US$574 million), the project is scheduled to begin construction in 2023 and be put into production by the end of the year. Tongwei said it will leverage its silicon and cell manufacturing footprint as it scales up module production. Tongwei's announcement comes after it revealed plans in September for a 25GW module manufacturing base in Yancheng, Jiangsu province, also representing an investment of RMB4 billion. The company aims to reach 80GW of module production by the end of 2023.

Qcells investing US$2.5 billion to establish US ingot, wafer, cell and module supply chain
Qcells plans to establish a fully integrated US solar manufacturing supply chain, aiming to manufacture solar ingots and wafers in the country as well as expand its module supply capacity. Qcells' parent company, Hanwha Solutions, said it intends to break ground on a 3.3GW of ingot, wafer, cell and module manufacturing plant in Bartow County, Georgia, in Q1 2023 and reach 8.4GW of module production in the state by 2024. The company is planning an expansion to its operations in Dalton, Georgia, to produce an additional 2GW of modules as well as its previously announced 1.4GW module fabrication plant in the state. The announcement constitutes an investment of around US$2.5 billion and was heralded by state Senator Jon Ossoff as the "largest" clean energy manufacturing investment in American history.

CubicPV to set up 10GW silicon solar wafer factory in the US
Solar manufacturer CubicPV is planning to establish a 10GW mono wafer manufacturing facility in the US that it said will be the "first of this scale" in the country. The plant would fill a void in the US PV manufacturing supply chain; the country has no domestic solar ingot, wafer or cell manufacturing capacity, according to research from the Solar Energy Industries Association published last year. The facility is expected to be fully ramped up in 2025.

Enel to build 3GW solar cell and module manufacturing factory in US
Enel North America intends to build a solar cell and module manufacturing facility in the US with an initial capacity of at least 3GW. The factory is intended to produce bifacial heterojunction PV cells, while the modules will have a tandem structure, utilising two stacked cells to capture more light than a single-cell structure, according to Enel. It said that the modules produced will be able to exceed 30% efficiency. Set to be built under Enel North America's subsidiary 3Sun USA, the factory will have a minimum manufacturing capacity of 3GW, and the company cites the potential to scale up to 6GW of production capacity annually. Enel is currently assessing potential locations for the factory, which is scheduled to begin construction in 2023, with the first modules available to the market by the end of 2024.

Canadian Solar to add 14GW of wafer and cell manufacturing capacity in China
CSI Solar plans to expand its solar and battery storage manufacturing capacity in China through an investment agreement with the municipal government of Yangzhou City in Jiangsu Province. The company – a subsidiary of Solar Module Super League member Canadian Solar – said it plans to add vertically integrated high-efficiency wafer, cell, module and battery storage production capacity under the agreement, to be deployed in three phases. The first phase, expected to begin production in the second half of this year, will add 14GW of annual wafer and cell production capacity. Canadian Solar said that the second and third phases of the agreement are subject to change and offered no construction or completion timeline. The company now foresees ending 2023 with 20GW of ingot, 35GW of wafer, and 50GW of cell and module capacity in light of this announcement.

Trina's 6.5GW Vietnamese wafer factory to be online this year, targeting US market
Trina Solar US has announced that its 6.5GW PV wafer manufacturing facility in Vietnam specifically designated to supply the US market will be online in mid-2023. The US arm of the Chinese solar manufacturer has confirmed that its module and cell production in Southeast Asia will use wafers produced at the Vietnam facility as part of its ongoing supply chain diversification in response to the US's ongoing anti-dumping/countervailing duty investigation. Trina said that it has already begun developing a supply chain with polysilicon sourced outside of China, with modules and cells manufactured in Southeast Asia. The wafer production facility will further diversify its supply chain, shoring up its compliance with the US's import laws and solidifying supply to the country.

EFFICIENCY AND PERFORMANCE

New wafer production method could double throughput, rendering European manufacturing more competitive
A research consortium has devised a proof of concept for a production line with a throughput of 15,000 to 20,000 wafers per hour, which is double the usual amount. The group of plant manufacturers, metrology companies and research institutions is being led by the Fraunhofer Institute for Solar Energy Systems ISE and was established to reduce production costs and alleviate supply bottlenecks as a means to deploy increasing amounts of solar. This would not only improve efficiencies and costs, the researchers said, but also render European manufacturing more competitive with China. New methods saw the researchers enact an 'on-the-fly laser equipment', which allows high-speed processing of

large wafers as they move under the laser scanner, as well as rotary screen printing instead of the current standard process of flatbed screening for the metallisation of solar cells.

HZB reaches 32.5% perovskite-silicon tandem cell efficiency, reclaiming world record

Helmholtz-Zentrum Berlin (HZB) has claimed a silicon-perovskite tandem cell efficiency of 32.5%, returning the record of the cell efficiency to the German research centre. The rate was certified by the European Solar Test Installation in Italy, as well as being included in the National Renewable Energy Lab chart of solar cell technologies, maintained in the US. The cell, consisting of a silicon bottom cell and a perovskite top cell, includes an interface modification to reduce charge carrier recombination losses. While the top cell can utilise blue light components, the bottom cell converts the red and near-infrared components of the light spectrum. HZB confirmed that the size of the test cell was 1.014cm².

JinkoSolar lays claim to n-type TOPCon cell efficiency record of 26.1%

JinkoSolar has laid claim to a new conversion efficiency record for a monocrystalline TOPCon solar cell of 26.1%. The record, independently confirmed by the National Institute of Metrology in China, was achieved using a 182mm n-type monocrystalline solar cell. According to JinkoSolar, its research and development department developed interface defect passivation, highly transparent polysilicon film and ultra-thin metallisation technologies based on a laser-doped selective emitter. Describing the record as a "major breakthrough" for the company's TOPCon cell technology in less than half a year from the previous record, JinkoSolar CTO Jin Hao said it also served as an "important milestone in the innovation of the company's products and solutions".

LONGi sets 26.81% efficiency record for heterojunction solar cells

Solar manufacturer LONGi has set a world record conversion efficiency level of 26.81% for silicon heterojunction (HJT) PV cells. Validated by the Institute for Solar Energy Research in Hameln, the record was achieved using mass production processes and full-size silicon wafers, according to LONGi. The milestone comes after the manufacturer reached 26.5% HJT cell efficiency last June, achieved on M6 full-size monocrystalline silicon wafers.

POLICY

'A significant moment for European solar manufacturers': EU unveils Green Deal Industrial Plan

The EU has announced a multi-pronged scheme to drive renewable energy and clean technology development, with the aim of putting the European market at the forefront of the global energy transition. The Green Deal Industrial Plan was unveiled in January by European Commission president Ursula von der Leyen in a speech at the World Economic Forum that directly positioned the plan as a response to both the Russian invasion of Ukraine and other global renewable energy legislative commitments like the US' Inflation Reduction Act. Von der Leyen said that the plan will cover four key pillars: the regulatory environment, financing, skills and trade. "The Green Deal Industrial Plan is a significant moment for European solar manufacturers. The EU is seriously acting on the concerns of the European solar sector over the last months and years," said Dries Acke, policy director of trade body SolarPower Europe.

Solar module imports nosedive in India following BCD tariff, JMK Research finds

Imports of solar modules in India decreased by 64% in Q3 2022 compared with the prior quarter whilst cell imports increased by the same amount, according to consultancy JMK Research. The drop is due to the introduction of a 40% basic customs duty (BCD) on imported solar modules. The BCD came into effect in April last year, imposing a 40% duty on module imports and 25% on solar cells in efforts to encourage domestic manufacturing and reduce dependence on imports. The JMK research also said that quarterly exports increased compared with the previous quarter's figures – cell and module exports were up by 57% and 524%, respectively.

MATERIALS

Daqo New Energy to increase Inner Mongolia polysilicon capacity by 100,000MT in 2023

Polysilicon producer Daqo New Energy has increased its expected polysilicon production capacity by 100,000MT in Inner Mongolia to reach a total production of 305,000MT by the end of 2023. Within its newly announced phase 5B polysilicon expansion project in Inner Mongolia for this year, Daqo expects to increase the capacity with an estimated capital expenditure of RMB9.2 billion (US$1.31 billion). Currently under construction in Inner Mongolia is phase 5A, which would add a capacity of 100,000MT and is expected to be completed during Q2 2023. Upon completion, the Inner Mongolia expansion phases 5A and 5B – each adding 100,000MT of polysilicon capacity – will contribute nearly two-thirds of the company's polysilicon capacity, according to Longgen Zhang, CEO of Daqo New Energy.

REC Silicon, Hanwha Solutions ink supply deal for polysilicon produced at idle US facility

Silicon materials producer REC Silicon has concluded a 10-year agreement with South Korean conglomerate Hanwha Solutions to offer fluidised bed reactor (FBR) polysilicon. The company's subsidiary REC Solar

Grade Silicon entered into a binding term sheet with Hanwha Solutions for a 10-year take-or-pay offtake for FBR polysilicon produced at an idle facility at Moses Lake, Washington. The offtake is to provide for the entire FBR production from the facility to Hanwha Solutions. "Securing offtake of production volumes has been a prerequisite for the reopening of the Moses Lake facility, and it marks a milestone to have this in place. We continue to move forward with our plan for a restart of the facility in Q4 2023 with an ambition to reach full capacity utilisation by the end of 2024," said Kurt Levens, CEO of REC Silicon.

Tongwei plans US$879 million silicon production facility in China

Tongwei held a signing ceremony in February for a 120,000-ton high-purity crystalline silicon project it plans to set up in China's Sichuan province. According to an agreement signed by the manufacturer and local authorities, the project will be located in Wutongqiao New Industrial Base, requiring an investment of around RMB6 billion (US$879 million). It is projected to start construction by the end of June 2023 and be put into operation in 2024. The annual output value after delivery from the plant will be about RMB20 billion (US$2.9 billion).

PEROVSKITES

European consortium begins perovskite-silicon tandem cell research project

Europe will benefit from a new research and innovation (R&I) project intended to advance the continent's tandem solar PV cell manufacturing and production capabilities, focusing on tandem silicon-perovskite cells. Entitled PEPPERONI, the project will run for four years and is co-funded by the EU under Horizon Europe – its long-term funding programme for R&I – and the Swiss Secretariat for Education, Research and Innovation. Coordinated by climate research institute Helmholtz-Zentrum Berlin and solar manufacturer Qcells, the PEPPERONI project began on 1 November. Qcells said that a pilot line for tandem production will be established at its European headquarters in Thalheim, Germany, aiming ultimately at industrial production of perovskite-silicon tandem cells. Over the four-year lifespan of the project, funding will total around €14.5 million (US$15 million).

Meyer Burger in partnerships to develop perovskite tandem technology, targeting industrial scale

Heterojunction cell and module manufacturer Meyer Burger has established a new series of partnerships to research and develop perovskite tandem solar technology, with a view to bringing the technology to industrial scale. The Switzerland-headquartered company will partner with the Swiss Centre for Electronics and Microtechnology (CSEM), Helmholtz-Zentrum Berlin, Fraunhofer ISE and the University of Stuttgart to pursue industrialised perovskite production and greater efficiency in future PV modules. Meyer Burger also said that, in partnership with CSEM, it has already achieved 29.6% energy efficiency for a 25cm2 perovskite tandem cell, by combining silicon heterojunction cells with perovskite structures.

SUPPLY DEALS

SC Solar supplying 5.2GW heterojunction module equipment line to Reliance Industries in India

Solar equipment manufacturer SC Solar has signed a 5.2GW heterojunction module automation production line supply agreement with Indian conglomerate Reliance Industries. The product being supplied to Reliance is the largest solar module production line in India, according to SC Solar, which said it is also the largest heterojunction line project in the industry. SC Solar's line of work is around research and development, manufacturing, sales and services of equipment in the solar industry. It works on TOPCon, heterojunction and perovskite solar cell and module technology.

First Solar secures module supply deals with Intersect Power, National Grid Renewables

US solar manufacturer First Solar will supply renewables developer Intersect Power with an additional 4.9GWdc of its thin-film PV modules. The transaction means that Intersect Power ordered 7.3GWdc of First Solar technology in 2022. The orders will go towards Intersect Power's pipeline of solar, storage and green hydrogen projects across the US between 2025-29, which will deploy First Solar's Series 6 Plus and Series 7 modules. The manufacturer has since entered into an agreement with developer National Grid Renewables to supply 1.6GW of its Series 7 modules, expanding the relationship between the companies to more than 4GW after they signed a 2GW supply agreement earlier last year.

Qcells pens 2.5GW solar module supply deal with Microsoft

Solar PV manufacturer Qcells has signed a deal with Microsoft to supply at least 2.5GW of its modules to projects from which the tech giant will purchase renewable energy. The company, a subsidiary of Korean conglomerate Hanwha, will provide modules and engineering, procurement and construction services for projects across the US where Microsoft has a power purchase agreement in place. The companies said that this agreement is the first of its type, where a power offtaker – one of the largest in the world – has established a relationship with a solar supplier, targeting projects from both upstream and downstream perspectives. Microsoft added that through this deal it hopes to drive the growth of US-made solar.

Product reviews

PV Modules: **LONGi**

LONGi's Hi-MO 6 module provides aesthetic appeal for distributed generation applications

Product outline: LONGi's Hi-MO 6 is the company's first module designed exclusively for the distributed generation market. Featuring hybrid passivated back contact (HPBC) cell technology, the range achieves a maximum efficiency of 22.8% in mass production while offering superior efficiency, safety and aesthetics.

Problem: Some homeowners and businesses are looking to benefit from rooftop solar systems but have concerns that panels will compromise the aesthetics of buildings.

System performance is impacted by low levels of irradiance and shading from trees or other buildings.

Solution: Responding to diverse customer needs in the distributed generation market, the Hi-MO 6 is available in four variants – Explorer, Scientist, Guardian and Artist – all of which are in the standard M10 size (182mm). While the range has a minimalist industrial design to complement a variety of applications, the Artist variant goes a step further with a host of customed sizes and colours, potentially of interest for buildings such as cultural sites or sports stadiums.

Modules equipped with HPBC cell technology can generate a greater volume of energy under high-temperature and low-irradiation conditions and also have superior power degradation performance. Under low light conditions, the high open voltage feature of the Hi-MO 6 enables it to reach the working voltage of the inverter more quickly.

The Hi-MO 6 also offers the option of further enhancing safety and optimisation by pre-installing the smart optimiser. In the event of a PV system failure or module shading, the back-end system may be remotely monitored and optimised using feedback from the smart optimiser's 'digital brain', ensuring system safety while maximising power output.

Application: Available for residential households and commercial and industrial sectors.

Availability: Available now.

PV Modules: **Tongwei Solar**

Tongwei Solar shingled modules offer high efficiencies and reliable power generation at competitive costs

Product outline: Tongwei Solar's shingled modules, built on 210 cells, are based on the company's innovative patented shingled technology, forming flexible interconnects and a unique internal circuitry, enabling higher efficiencies and better power generation performance. The maximum power of a single module can now reach 670W and efficiency has been enhanced to 21.6%.

Problem: With the rapid development of renewable energy sources around the world, land resources available for projects are becoming increasingly scarce. This requires PV systems to maximise power generation and efficiency in order to achieve maximum return on investment from each project.

During module operation, the risk of hot-spots not only affects power output but also causes safety risks, potentially reducing module durability.

The solder ribbons inside the modules contain lead, which can cause environmental pollution.

Solution: In comparison to other module BOS costs, Tongwei's shingled modules feature higher power. Their utilisation of bracket, pipe pile and cabling is higher, resulting in a reduction in construction cost per watt and, logically, lower levels of investment.

Compared to conventional modules, shingled modules involve a cell cut into strips. The technology results in both string current within the module and the risk of hot-spots being lower.

Shingled modules use shingled bonding technology instead of connection via solder ribbons, so lead content is also significantly reduced. Testing has shown that Tongwei's shingled modules are resistant to extreme weather conditions and perform better under shading, resulting in extended working life and service condition.

Application: Household, commercial and industrial and centralised systems.

Availability: Currently available.

PV Modules: **Yingli Solar**

Yingli eyes residential, commercial PV sectors for its new YLM 3.0 Pro module

Product outline: Yingli Solar's new YLM 3.0 Pro 415W module is ideal for both residential installations and commercial projects where larger, more cumbersome modules are difficult to site efficiently around typical obstacles found on many commercial buildings. A smaller footprint combined with a high module efficiency of 21.3% enables superior energy density in many cases.

Problem: Modules seem to be continuously getting bigger and more difficult to handle, especially on windy days. Global issues are resulting in shipping and freight prices increasing. Staff shortages have also had a detrimental effect on logistics and product delays, while the cost of energy is escalating rapidly.

Solution: The Yingli Solar YLM 3.0 Pro 415W module has been specifically designed to address a sweet spot in the market, blending a physically smaller footprint with a high-power efficiency that requires fewer panels and less roof space to maximise energy production.

This smaller footprint also drastically reduces the number of containers needed to be shipped per megawatt, pallets to be processed by logistics staff and panels that need to be installed on a total kilowatt basis.

This product comes with 1200mm leads and Evo 2 connectors (1500V version of the genuine MC4) to enable a simple and quick installation when using mainstream brands of optimisers or microinverters. The black frame also enhances the overall look of the completed system where aesthetics is an important factor.

All modules have both a 25-year product warranty and a 25-year performance warranty irrespective of where it is installed.

Applications: Residential and commercial markets.

Platform: At 1722 x 1134mm in size and weighing 21.5kg per module, the compact size and weight make the module easy to install for rooftops of all sizes.

This product has further advantages including:

- Higher durability: The multi-busbar design can decrease the risk of cell micro-cracks and conductive fingers fracturing. Multi-busbars reinforce the cell and reduce resistance.
- Half-cell design: Less energy loss through shading due to a new cell string layout and split J-box, and lower cell connection power loss using a half-cell design.
- The cells have a gallium-doped structure that improves high-temperature performance and stability.

Availability: The new 415W solar panel is now available across Australia.

A boost for edge passivation of TOPCon and SHJ solar cells

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Abstract

Currently, the mainstream product of the photovoltaic industry is the PERC cell and its half-cell modules, which are connected in series by metal wires to form module panels. However, since PERC efficiency has plateaued, the next-generation industrial products in passivation contact technology, such as TOPCon and SHJ cells, will eventually replace PERC cells as the market's preferred option. An alternative method of module assembly is to cut these highly efficient cells into half-cells, multiple half-cells or "shingle panel modules". However, the main hurdle to the upgrading of the new technology is the large performance losses that high-efficiency TOPCon and SHJ cells suffer during the cutting and separating process for the assembly of shingle panels. For example, when a complete SHJ cell is cut into tenths, its efficiency decreases from 24.7% to 22.7%. This issue is significantly limiting the urgent industry upgrading of PERC to TOPCon and SHJ. Recently, a collaboration between DAS Solar and Chen Group applied a spraying approach to form an organic passivation film on the lateral side of cutting cells, to compensate for the cutting losses of the two types of high-efficiency cells.[1] This passivation-liquid-based method can be easily integrated into the current production line and thus solve the problem of efficiency losses. This paper reviews the idea and methodologies of the passivation-liquid-based compensating technology for the separation loss of silicon cells, which provides future perspective for the photovoltaic industry and potentially helps to promote industry upgrades.

Introduction

Crystalline silicon cells (c-Si) are currently the dominant technology with over 95% market share. Because the rear silicon surface alloyed with aluminium (Al-BSF) can lead to high carrier-recombination velocity and poor reflection, the PV industry switched from Al-BSF cells to PERC cells from 2013 onwards. By the end of 2020, PERC occupied more than 80% market share[2] Meanwhile, half-cell modules that can reduce power dissipation in the cell interconnection and enhance power outputs have been used in combination with PERC technology on a large scale.[2] However, as technology advances, the efficiency of commercially mass-produced cells based on PERC has plateaued.[3] Typically, the direct utilisation of metal on a silicon wafer will lead to a significant recombination loss. Therefore, passivating contacts are being developed to further reduce contact recombination losses and improve mass-production efficiency.[4–7] Depositions of dielectric passivation layers such as hydrogenated amorphous silicon nitride (a-SiN_x:H), and amorphous hydrogenated silicon (a-Si:H), SiO_2,[8] Al_2O_3[9] and their stack layer[10–12] are used for the silicon solar cells to suppress the carrier recombination at their surfaces. Thanks to these passivation techniques, TOPCon,[13] SHJ[14] and Interdigitated Back Contact (IBC)[15] have emerged as the most promising next-generation PV cell technologies. Furthermore, a half-cell module and shingle module can generate higher power than a full-wafer module in a limited area, and thus can be combined with passivating contact cell technologies to further improve the mass-produced cell efficiency. Specifically, a shingle panel module has the following advantages: (a) it produces more energy; (b) it can be wired in groups and configured in parallel to reduce losses caused by shading; (c) it reduces the hotspot effect and increases the life of the module[16]; and (d) it reduces the risk of component cracking.[17–18] In short, shingle solar panels can fabricate modules with high density and high PCE and reduce cell-to-module (CTM) losses.

For the integration of stripes into shingle solar panel modules, it is necessary to cut the host/complete silicon cells into halves, thirds, quarters or even more sub-cells through a laser-scribing process,[19] which will inevitably cause cutting damage and form new unpassivated edge surfaces, leading to a large decrease of PCE due to recombination.[20–21] The combination of water and thermal laser separation (TLS) is currently used to solve the problem of cutting damage from the conventional laser-scribing and mechanical cleaving process. However, the unpassivated silicon on the new cross-sections created by cutting is still a problem that needs to be solved. Baliozian et al.[20, 19] solved this problem by depositing an Al_2O_3 layer using atomic layer deposition (ALD) along with a light-soaking process. However, ALD technology is expensive and complicated and, more importantly, ALD-deposited Al_2O_3 is incompatible with the thermal laser-separation process (cutting water) used on production lines.

In order to advance to the next generation of silicon solar cells, a simplified passivation technology is urgently required. It should meet the requirements of: (i) a high-quality passivation effect; and (ii) vacuum-free, room temperature processes as well as not requiring post-annealing. In this regard,

Cell type	PCE	Cut side by laser	ΔPCE	ΔUoc/mV	ΔIsc/mA	ΔFF
TOPCon	22.6%	Front	−0.231	−1.3	−18.3	−0.523
		Rear	−0.170	−1.1	−14.1	−0.363
	23.0%	Front	−0.202	−1.1	−17.2	−0.444
		Rear	−0.217	−1.0	−16.2	−0.520
	23.4%	Front	−0.246	−1.0	−20.0	−0.583
		Rear	−0.259	−1.0	−19.9	−0.629
PERC	22.4%	Front	−0.237	−2.4	−2.0	−0.560
		Rear	−0.260	−1.7	7.0	−0.792
	22.6%	Front	−0.244	−2.4	1.0	−0.594
		Rear	−0.267	−3.0	6.0	−0.647
	22.9%	Front	−0.163	−2.3	5.0	−0.342
		Rear	−0.253	−2.0	10.0	−0.748

Table 1. Cutting losses referring to the decrease in performance of solar cells after being cut by a traditional thermal laser, compared to their performance before cutting. Measured values are obtained under standard test conditions (STC) of 25°C, 1000w/m² and AM 1.5G, which are industry-standard testing conditions for solar cells. Cells are tested by exposing them to laser incident from either the front (for TOPCon cells it is a p+ emitter, while for PERC cells it is an n+ emitter) or the rear.

the new passivation technology will revolutionise the current production process of industrialised crystalline silicon cells and simplify the passivation of silicon materials.

This paper presents an overview of passivation-liquid-based compensating technology as a new solution for next-generation shingle modules of TOPCon and SHJ cells, as well as describing methodologies for the study of this new technology, the mechanisms of the passivation stability and compatibility with production lines.

New solution-based passivation technology: electrochemical passivation

As the core of silicon PV devices, high-temperature or vacuum-processed thin dielectric passivation films are facing technological complexities that hinder industrial transformation. Most notably, the current passivation technologies are unable to solve the edge recombination issues of shingling solar cells induced by the separation, which is currently the main module technology in the PV industry. Dielectric passivation films, such as Al_2O_3, have been used to try to solve this issue. For example, Munzer et al. combined ALD Al_2O_3 with subsequent light-soaking to passivate edge surfaces, and proved the beneficial effect of side passivation on half-cells and half-cell modules.[19] However, the problem was not fully solved because it is not easy to selectively perform the vacuum-processed passivation technology only on the newly cut section. In addition, it requires additional post-annealing, and it is also an inconvenient operation and less cost-effective. Therefore, a new and more feasible passivation technology is required.[22–23]

Recently, Chen et al. developed a passivation scheme involving organic thin films that rivals traditional dielectrics and, most importantly, is a solution-based passivation technology.[24–26] The method is reliant upon spin-coating polymers with a sulfonic functional group (–SO3H) and the ability of these to spontaneously form sub-oxides (Si-O-R) at the silicon surface.[26–27] This solution-processed passivation scheme can achieve an effective minority carrier lifetime of 9.6–28.6 ms and is in line with hydrogenated amorphous Si or SiO2 film-passivation schemes currently used in the PV industry.[25–26] Unlike conventional chemical passivation or field-effect passivation, the electrochemical grafting passivation of silicon via electron transfer at the polymer/silicon hybrid interface is thought to be responsible for the passivation mechanism. Based on this electrochemical passivation, the interface state is switchable, with the feature of enhanced passivation due to external conditions, such as an O2 atmosphere or an applied bias voltage. To date, polystyrenesulfonate (PSS), poly(2-acrylamido-2-methylpropanesulfonic acid) (PAMPS), polystyrene-block-poly(ethylene-ran-butylene)-block-polystyrene-sulfonated-cross-linkable (PS-b-PERB) and Nafion have been used for this purpose.[24–26]

The technical features of this type of solution-based passivation technology can be summarised in the following five points: (i) the origin of passivation is based on the functional group; (ii) the passivation mechanism is electrochemical; (iii) the passivation effect can be controlled by electron transfer at the Si surface; (iv) it has the potential to be intrinsically low cost due to the organic materials and low-temperature and high-vacuum-free processing; and (v) it can perfectly match the edge passivation of cut-cells.

Cutting loss

Table 1 shows the cutting losses of PV parameters of industrial TOPCon and PERC cells by traditional thermal cutting. Recently, a new TLS technique has been developed, which consists of generating

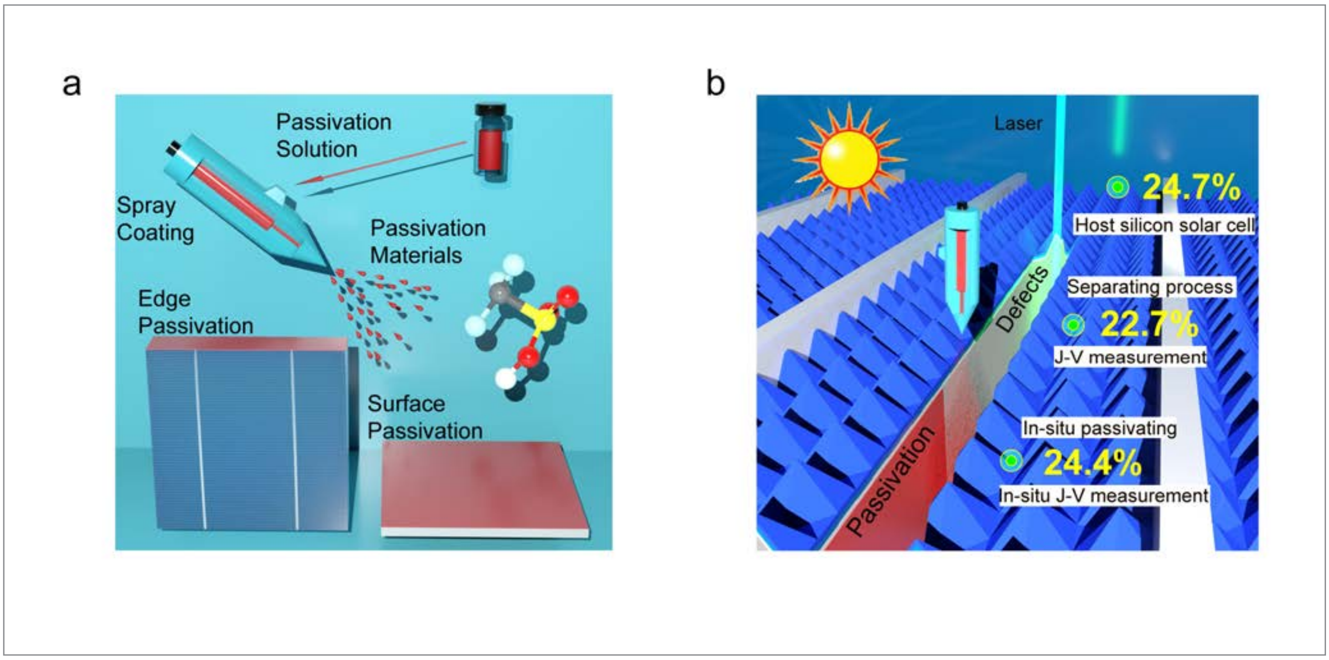

Figure 1. (a) Schematic of spraying organic passivation agent on to edge surface of silicon solar cells and surface of silicon wafers. (b) Illustration of defect formation process caused by laser-cutting separation and repair by passivation solution treatment.

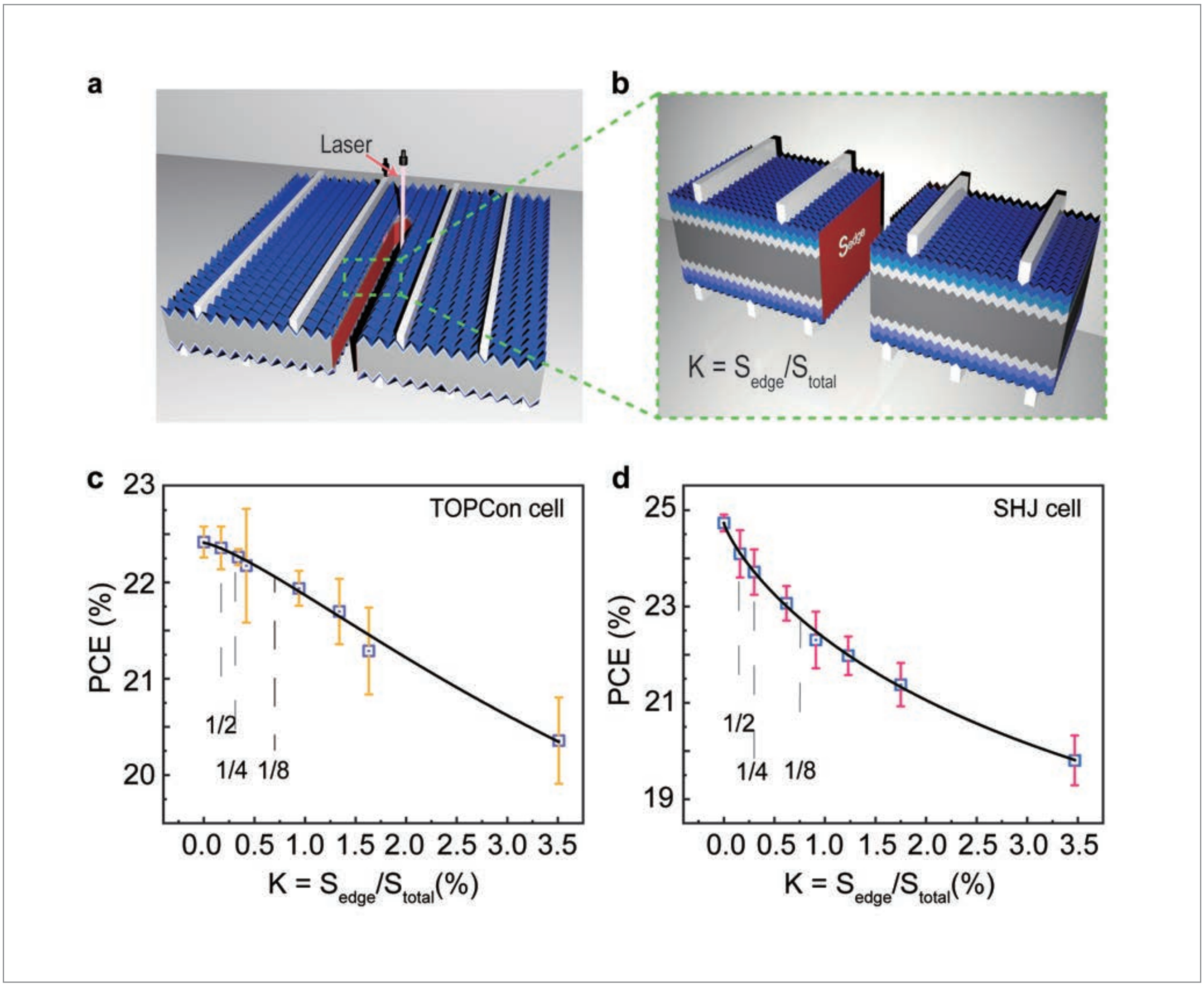

Figure 2. (a) Illustration of the cutting separation process of solar cells. (b) Schematic diagram of the ratio of defect area to the solar cell total area ($K = \frac{S_{edge}}{S_{total}}$). Statistical graphs of the different degrees of efficiency loss caused by the shingling process of two commercial crystalline silicon cells, namely (c) TOPCon and (d) SHJ.

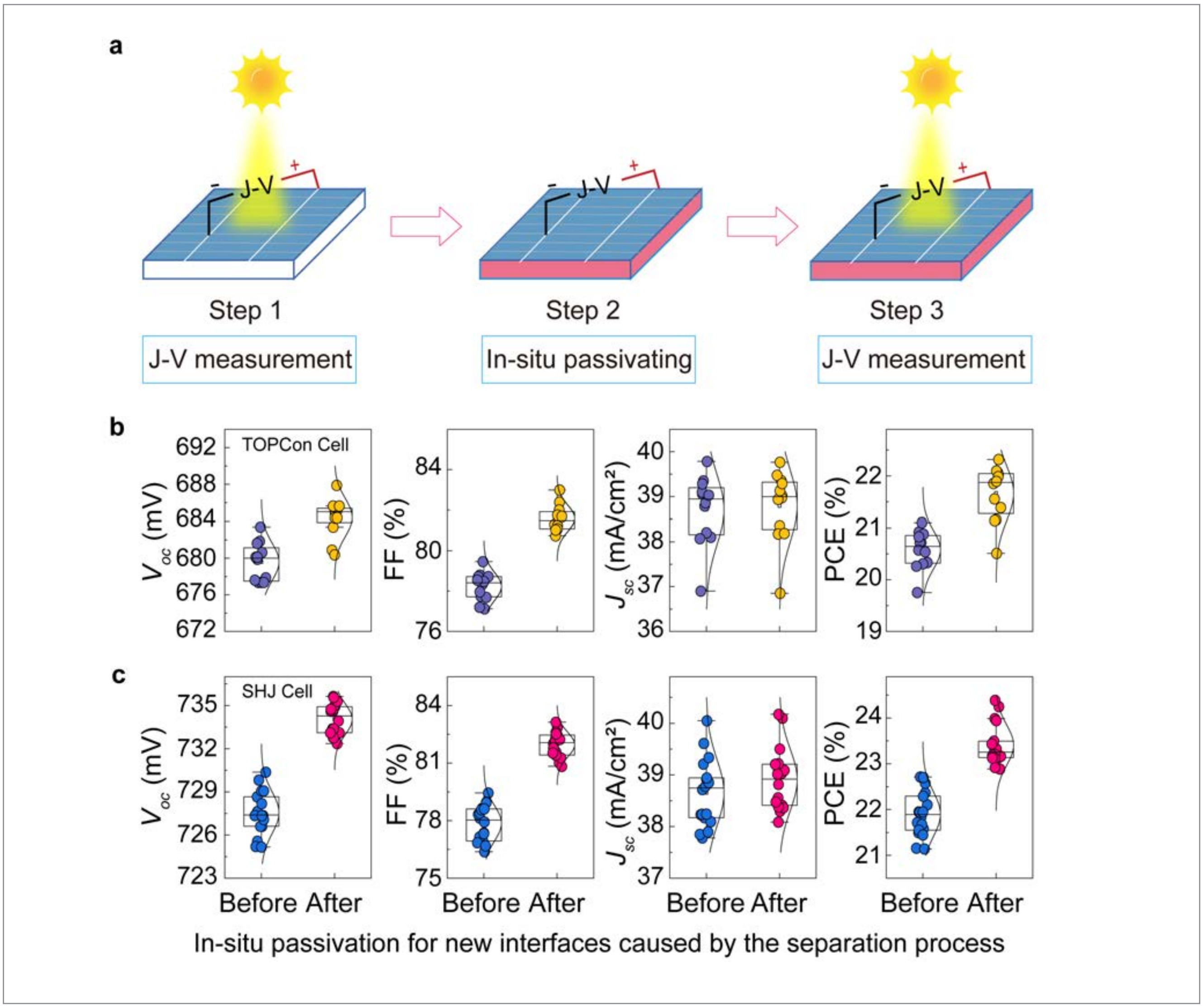

Figure 3. (a) Schematic diagram of J-V characteristics for in-situ edge passivation of the optimised SHJ devices. (b–c) Box statistics of device parameters before and after passivation of TOPCon and SHJ solar cells.

compressive and tensile stresses along the separation path by means of a thermal gradient, which is the result of the combination of a hot laser source and a cold-water–air-aerosol cooling jet. When the cell is cut in half, the cutting loss of PCE in a PERC cell remains around 0.1% but, for TOPCon cells, the loss of PCE can be up to 0.2%.

Solving edge-passivation issues

The solution-based passivation technology is fully compatible with the current production line by simply changing the water for TLS technology to a passivation solution. The organic passivation coating can substantially reduce the newly formed edge loss from laser-scribing. For example, after edge passivation using a Nafion passivation liquid, both types of c-Si cells (TOPCon and SHJ) have absolute efficiency improvements of 0.5–2% and a power enhancement of 3–5 W in the 1/10 sub-cells. As a result, the best PCE performance on the 1/10 SHJ cells has increased from 22% to 24.38% (Figure 1).

Methodologies

1. Definition of edge recombination dependence factor

Before the study of compensating for cutting losses, a systematic scheme is necessary. When a full-cell is cut into several sub-cells, recombination at the newly created unpassivated edges after cutting would lead to a decrease in open circuit voltage (V_{oc}), fill factor (*FF*) and PCE of solar cells.[20–21] To evaluate these cutting losses, Chen et al. define the ratio of the newly formed edge area (the cross-sections by separation process) to the total area (all surfaces) as K ($K = \frac{S_{edge}}{S_{total}}$) (see Figure 2).[1] When TOPCon and SHJ cells are separated into different sizes, the PCE as a function of K is calculated, as shown in Figure 2 (c–d). As the value of K increases, the efficiency of the two types of devices gradually decreases, indicating that the new side surfaces lead to high recombination losses. Especially for SHJ cells that have higher efficiency, the PCE drops approximately

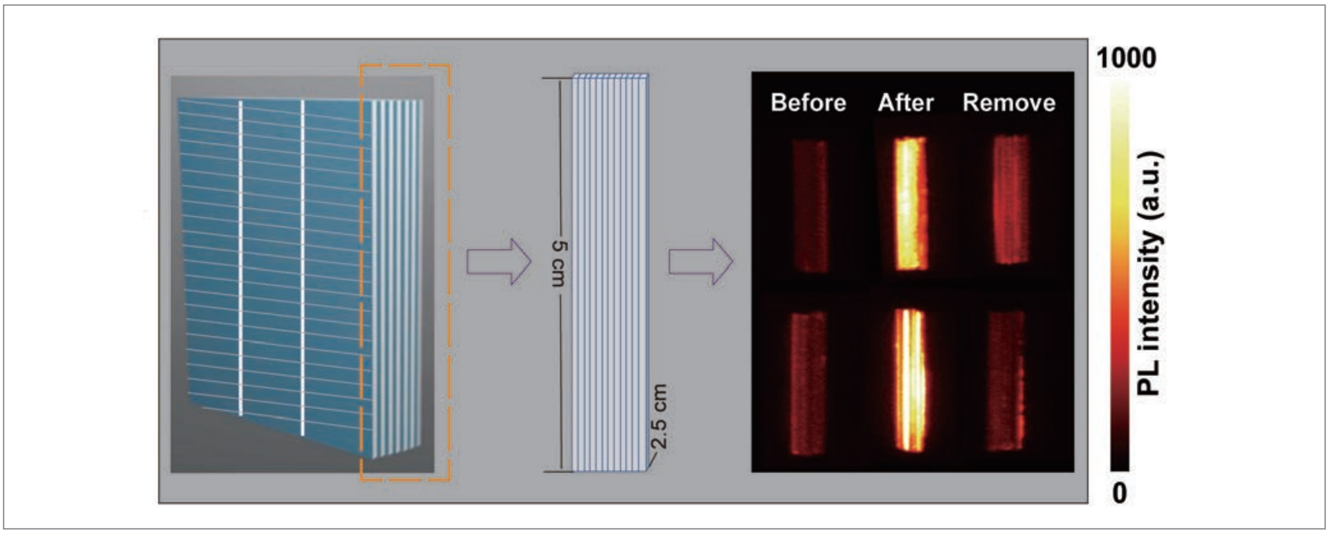

Figure 4. Schematic of the edge situation of multiple-piece stacked TOPCon and SHJ silicon solar cells, along with a PL mapping image of TOPCon and SHJ solar cells with/without edge passivation.

exponentially.

2. In-situ passivation and in-situ characteristics of PV parameters

When a cell is separated into many smaller sub-cells, the measurement of PV performance on the production line becomes a problem due to mismatched tools. The differences in PV parameters between the mother cell and sub-cells are small; in this case, if the excellent edge passivation is used, it is difficult to observe the differences accurately. In order to solve this problem, an in-situ passivation and in-situ characteristics method is employed. A schematic flow diagram of the in-situ passivation is shown in Figure 3. By analysing in-situ measurements of 18 samples, the V_{oc} was found to increase by 5.5±2.5 mV and 7.5±2.5 mV for TOPCon (K = 1.198%) and SHJ (K = 1.186%), respectively. The *FF* was also largely improved by 3–6%. Here, using a simple edge passivation technology, it was shown that *FF* can be increased from 77.9% to 82.5%. The average efficiency of all solar cells can be enhanced by 1–2% after the organic passivation.

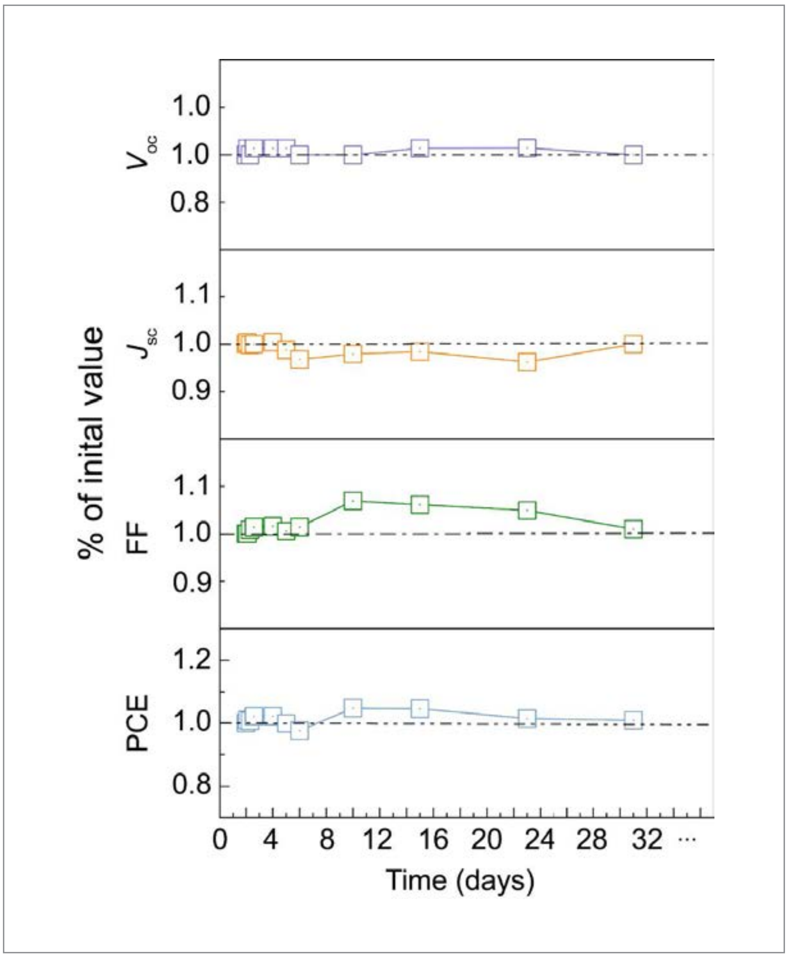

Figure 5. Stability of device parameter tracking after encapsulation of passivated SHJ cells.

3. Edge PL mapping

Figure 4 illustrates the edge situation of multiple-piece cut-cells stacked together after acquisition of cutting and photoluminescence (PL) mapping data of cut-cells with/without the liquid passivation coating. By comparing the PL mapping intensity before and after passivation, it can be seen that the solar cells with the passivation layer are brighter than without the passivation coating. This demonstrates that the coated passivation layer formed at low temperature by the spraying method has an excellent edge passivation effect for different commercial silicon solar cells, which is beneficial for relieving the edge recombination loss, increasing V_{oc} and enhancing the power of the modules. Next, we utilised a solvent to remove the passivation layer and the PL mapping is comparable to the result without passivation. This provides new options for wafer inspection without wasting wafers.

Stability issues

The long-term stability of Nafion has been discussed in previous work. For example, Qian et al. reported that Nafion-covered carbon nanotube (CNT) film has durable sheet resistance of more than 600 days and Nafion-applied CNT-Si solar cells showed excellent stability under a constant UV light for over 300 hours.[28] Chen et al. summarised that the increased stability of the electrochemical passivation is a result of an oxygen-enhanced and water-degraded operating mechanism,[24, 29] and it was confirmed that the appropriate encapsulation can prolong a device's stability for over 430 days.[29] A simple encapsulation was performed on the side-passivated SHJ device and its stability was tested, as shown in Figure 5. It can be seen from the analysis that the encapsulated device can maintain the passivation effect for a long time.

Summary and outlook

It is predicted by PV InfoLink[30] that TOPCon cells will see rapid development over the next five years and the capacity will expand up to 278 GW. This will stimulate demand for these modules with higher power. Thus, edge passivation will become very important to this industry. Here, we reviewed a low-temperature passivation solution technique that effectively solves the problem of efficiency loss caused by edge recombination in the CTM process. Importantly, this straightforward and non-vacuum method is compatible with current production lines and can be directly applied to industrial silicon solar cells in the future. Without requiring additional capacity investment, it has the potential to gain at least 1 GW while recovering $2.4 million in losses.

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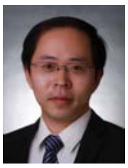

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Dr. Dengyuan Song has served as chief technology officer at DAS Solar since 2022, leading R&D into high efficiency crystalline Si solar cells and the technology of mass production. He has more than 35 years of experience in the R&D of solar cells, silicon materials and semiconductor photovoltaic devices. Prior to joining DAS Solar, Dr. Song was CTO at Yingli Solar. He is president of the SEMI China PV Standards Technical Committee and has published and presented over 260 papers in scientific and technical journals and at various PV industry conferences. He received his Bachelor's degree in Microelectronics Engineering from Hebei University, his Ph.D. in Photovoltaic Engineering from the University of New South Wales in Australia and is co-inventor on 42 patents.

Jianhui Chen obtained his Ph.D. at Hebei University in 2017 and is a member of Hebei province's Science Foundation for Distinguished Young Scholars and China's National Natural Science Foundation (NSF). He is currently Group Leader at Hebei Photovoltaic Technology's Collaborative Innovation Center, where he discovered the electrochemical passivation mechanism of silicon surfaces. He currently focuses his research interests on organic-inorganic interface physics and its related electronic devices and applications, incorporating organic passivating contact for silicon solar and related tandem solar cells, low-dimensional/organic composite materials and organic-inorganic hybrid interface memories.

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Development of HJT technology in China

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Abstract

In this paper, three generations of silicon heterojunction (HJT) solar cell technical routes in China are reviewed. We define the structure of HJT cells with an amorphous silicon thin film on two surfaces of a monocrystalline-silicon (c-Si) wafer as HJT 1.0, which is the first generation of HJT. HJT cells with silicon-oxygen thin film on the front side of a c-Si wafer are defined as HJT 2.0, and HJT cells with a silicon-oxygen structure on the front side and a microcrystalline silicon structure on the back side are defined as HJT 3.0. HJT 1.0 and 2.0 have been mass produced in China since 2021. Generation 3.0 will be going into mass production in the next two years. Several other advanced technologies also support the continuous cost reduction and efficiency improvement of HJT cells, such as new metallization technologies based on high mesh count screen plates and silver-coated copper paste, thin wafer technology, and new module technologies based on novel encapsulation materials. Huasun established a 500MW HJT 1.0 cell and module production line in 2021, with a 2GW HJT 2.0 cell and module production line following in 2022. Huasun set up an R&D laboratory in 2021 to conduct in-depth research on HJT 2.0 and HJT 3.0 technologies in order to promote the industrialization of HJT 2.0 and HJT 3.0 through collaboration with other companies, such as Maxwell.

Introduction

Photovoltaic technologies are in a stage of rapid development. On the one hand, the majority of market share has been taken up by conventional passivated emitter rear contact (PERC) cells with a superior economic performance. New cells, on the other hand, based on advanced technological routes, are progressively making their way into mass production. Among them, silicon heterojunction (HJT) cells, as a novel technology, have attracted the attention of the market for their high efficiency.[1]

Currently, n-type silicon wafers are mainly used for mass-produced HJT cells. Cleaning and texturing, silicon-based film deposition, transparent conductive oxide (TCO) film deposition and metallization are the four steps in producing HJT. During the cleaning and texturing stage, wafers are placed in an alkaline solution containing organic additives to remove surface dirt, etch saw damage and form a pyramid structure that reduces reflection. Deposition of silicon-based thin films is generally accomplished via chemical vapour deposition (CVD). Intrinsic amorphous silicon layers are deposited on both surfaces of the substrate to passivate the silicon surface. Doped silicon-based thin films are then deposited to create a built-in electric field.[2] Physical vapour deposition (PVD) is commonly applied for the deposition of TCO films, which protect silicon-based films and laterally conduct the electrical current as a transparent conductive electrode. Metallization is typically carried out by screen printing. The paste is printed on TCO films and then annealed in a furnace to dry the paste and solidify the grid lines. The efficiency is further improved after light soaking.[3]

World records for the efficiency of HJT cells have been set in recent years by numerous companies. In November 2022, the efficiency of LONGi HJT cells was verified by the Institute for Solar Energy Research in Hamelin (ISFH) to be 26.81%, setting a new record for HJT, which was the first time that a Chinese solar technology company had broken the record for silicon solar cells. This further demonstrates the technical superiority and market potential of HJT.

In this paper, we concentrate on the evolution of the internal structure of HJT and the current status and application of new materials and technologies, taking the large-scale manufacturing process of HJT at Huasun as an example to introduce the development of the product in China. Anhui Huasun Energy Technology Co., Ltd. was established in July 2020 and is located in Xuancheng City, Anhui Province. The company is dedicated to the production of and research into HJT, and has become one of the leading suppliers of HJT products in China with the world's largest HJT production capacity.

The evolution of the HJT structure

The structure of HJT determines the maximum possible absorption of sunlight and the effective collection of photogenerated carriers in the whole solar cell, which are key elements in determining photoelectric conversion efficiency. The technical route of the HJT cell is divided into three main generations, as shown in Fig. 1.

First generation: HJT 1.0

Fig. 1(a) illustrates the structure of mainstream HJT in the market up to 2019. The overall structure is Ag/TCO/n-a-Si:H/i-a-Si:H/n-c-Si/i-a-Si:H/p-a-Si:H/TCO/Ag, where n-a-Si:H is on the front side, and the p-n junction is located on the back of the cell to reduce light absorption of the p-a-Si:H. In this paper, an HJT cell with this amorphous silicon structure on both surfaces

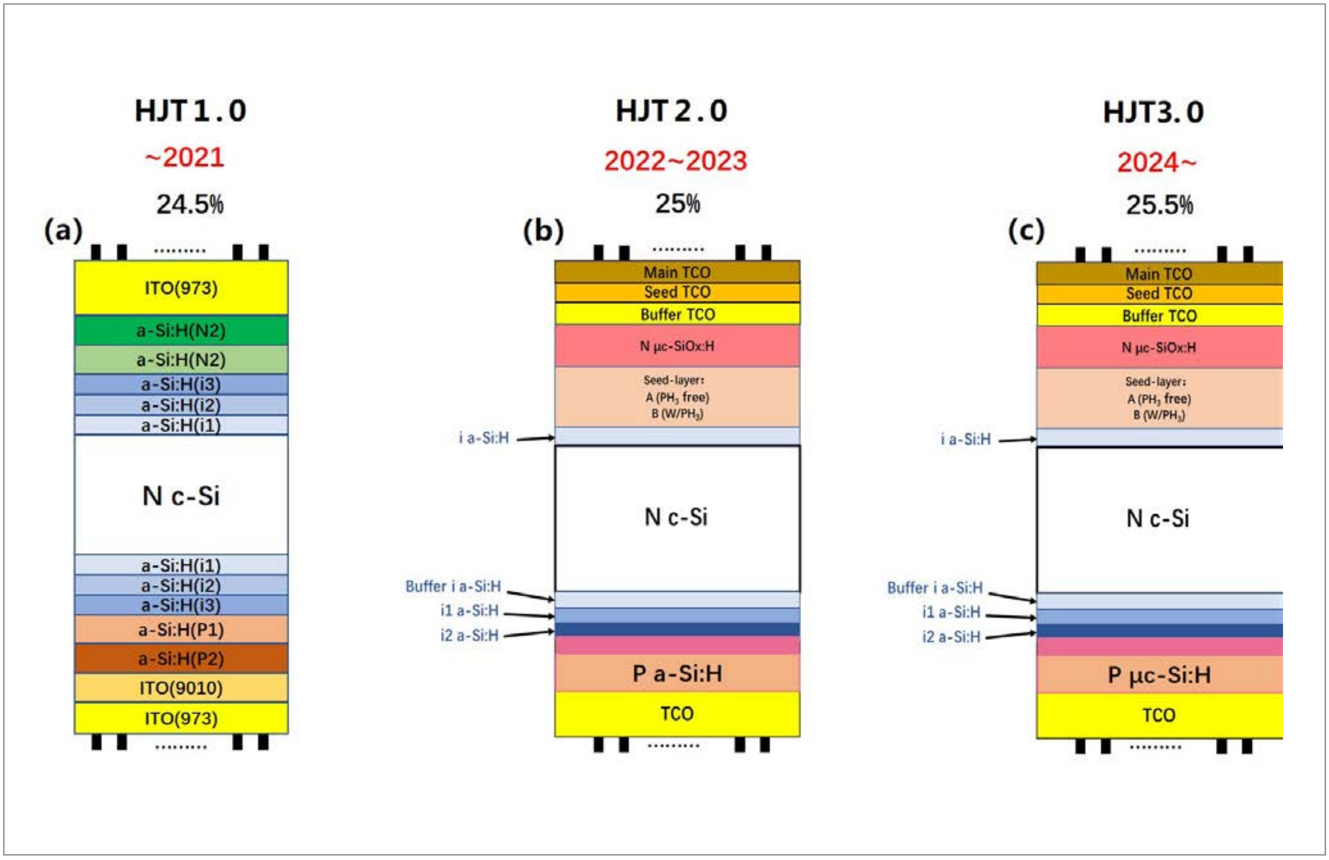


Fig. 1. Three generations of HJT technical routes

is referred to as HJT 1.0. The individual layers of these films can also be further separated and optimised in accordance with equipment conditions or production requirements. In Fig. 1(a), the i-a-Si:H films on the front and back surfaces are divided into three layers. The i1 + i2 stack is a thin composite buffer layer with a high percentage of dihydride (Si-H2) bonds.[4,5] It effectively inhibits epitaxial growth[6] and passivates the substrate surface. In addition, the i3 layer is a dense passivation layer[7,8] in which monohydride (Si-H) bonds dominate.[4,5] n-a-Si:H and p-a-Si:H films are also divided to form a gradient-doped structure. This improves contact between intrinsic and doped silicon-based film, as well as between the doped silicon-based film and TCO. Composite films are used in TCO to achieve high efficiency and low cost,[9] such as the bilayer of ITO-90/10 (In2O3:SnO2 = 90 wt.%:10 wt.%) and ITO-97/3 (In2O3:SnO2 = 97 wt.%:3 wt.%) in Fig. 1(a). ITO-90/10 and a-Si:H have strong electrical compatibility, and ITO-97/3 has a higher deposition rate and a lower material price than ITO-90/10. The bilayer is a good balance between electrical properties and the cost of manufacture. After optimisation, the efficiency of mass-produced HJT 1.0 can reach 24.5%.

Second generation: HJT 2.0

At present, companies have successively entered the HJT 2.0 mass-production technology route to increase short-circuit current density. From the equipment side, very-high-frequency (VHF) excitation generally replaces radio-frequency (RF) excitation in plasma-enhanced chemical vapour deposition (PECVD) for amorphous silicon film microcrystallization. The structure of HJT transforms from n-a-Si:H on the front side into n-μc-SiOx:H. The optical band gap of n-type silicon-based film becomes wider and the light parasitic absorption is reduced as a result. [10] Additionally, the effective doping ratio of phosphorus is increased, so the built-in electrical field is strengthened via microcrystallization. TCO is also split into layers that contain the buffer layer, seed layer and the main function layer, to enhance contact with n-μc-SiOx:H and with grid lines. Combined with the matching and optimisation of other films, mass-production efficiency has been increased to more than 25%.

Third generation: HJT 3.0

Over the next one or two years, it is anticipated that the mass-production technical route for HJT will enter HJT 3.0. In contrast to HJT 2.0, the p-a-Si:H layer on the back side of HJT is also microcrystallized to form p-μc-Si:H.[11] The effective doping rate of boron is also greatly increased in microcrystalline silicon, similar to phosphorus. Therefore, microcrystallizing the p-type silicon-based film can improve the conductivity of layers, as well as enhance the built-in electrical field. With further optimisation, the cell efficiency of HJT 3.0 can surpass 25.5%.

No.	Item/test data	Power loss	I_{sc}	U_{oc}	*FF*
1	Original data	/	/	/	/
2	DH 1000h with 6A	−0.18%	−0.43%	0.30%	−0.05%
3	DH 2000h with 6A	−0.76%	−1.26%	0.29%	0.21%
4	DH 3000h with 6A	−1.28%	−1.82%	0.33%	0.22%
5	Place 50 day	−2.02%	−1.82%	0.05%	−0.26%
6	DH 6400h	−2.85%	−0.45%	−0.39%	−2.00%

Table 1. Damp-heat (DH) testing of modules based on Ag-coated Cu paste at Huasun (U_{oc} = open-circuit voltage, I_{sc} = short-circuit current, *FF* = fill factor)

In addition, cleaning and texturing and metallization processes should also be tailored to each technical route. For instance, different CVD technologies may require altering the size of the pyramids. In order to match the requirements, the texturing time and alkali and additive concentrations should be adjusted. The furnace temperature needs to be regulated since cells with different film structures have varied temperature tolerances. Different light-soaking parameters result in varying degrees of improvement for cells with different structures, necessitating appropriate modification.[12]

Advanced HJT technologies to achieve efficiency improvement and cost reduction

Designing and enhancing the HJT internal structure is key to increasing efficiency. In addition, numerous other advanced technologies are capable of further increasing the efficiency and stability of HJT, or reducing manufacturing costs.

New metallization technologies

The two major components of new metallization technologies are the screen plate and paste. In general, to a limited extent, increasing the mesh count in the rapid printing of high-viscosity silver paste can dramatically reduce silver paste consumption without compromising cell efficiency. At present, screen manufacturers promote 480 mesh count screen plates as their primary high mesh screen products. By appropriately adjusting printing parameters, improved grid line characteristics can be acquired while maintaining the same silver paste consumption, thus increasing efficiency. Besides silicon, silver paste has always been one of the most expensive components in HJT manufacturing costs. Reducing the quantity of silver will effectively reduce the cost of HJT. The application of silver-coated copper paste can replace silver with copper, which has become a specific cost-reduction strategy for HJT. It is specific to HJT since silver-coated copper paste can only be used in the region for low-temperature paste to prevent the silver coating from being damaged. Huasun has conducted trials on silver-coated copper paste from several manufacturers. The efficiency of printed cells is close to that of silver paste printed cells, and the grid line tensile strength and electrical performance stability (as shown in Table 1) are also excellent. It is expected that, in 2023, some companies will begin to fully use silver-coated copper paste instead of silver paste, reducing the silver consumption of a cell to 80 mg, which is consistent with PERC cells and completely solves the problem of high silver consumption.

Thin wafer technology

At the moment, the high cost of silicon wafers poses challenges for cell and module manufacturers. As a result, thin wafer technology is a method to considerably reduce costs. Fig. 2 depicts the electrical performance of cells that are made from wafers with different thicknesses using the same process. Clearly, the open-circuit voltage (U_{oc}) increases as wafer thickness decreases. This stems from the reduction of bulk recombination[13] with the thinning of the silicon wafer. However, the short-circuit current (Isc) and fill factor (FF) both decrease in line with decreasing wafer thickness due to the reduction in light absorption. There is no significant change in the efficiency of cells with thicknesses of 100–150 μm, it being evident that appropriately thinning the wafer does not lead to a decrease in cell efficiency. For the sorted cells with the same efficiency level, the power of a module composed of cells with a thickness of 130 μm is 0.16% greater than that of cells with a thickness of 150 μm, meaning that the module has a better cell-to-module (CTM) ratio. The cell efficiency is still 24.9% when the thickness is 70~80 μm and the cell can be bent properly, thus providing conditions for the future production of flexible HJT modules. Some HJT manufacturers now have their own silicon wafer department, providing thin silicon wafers for cell manufacturing. During the next one or two years, the silicon wafers used to produce HJT cells will be thinned to 130 μm. Of course, thin wafer technology will face a challenge in the case of automated systems.

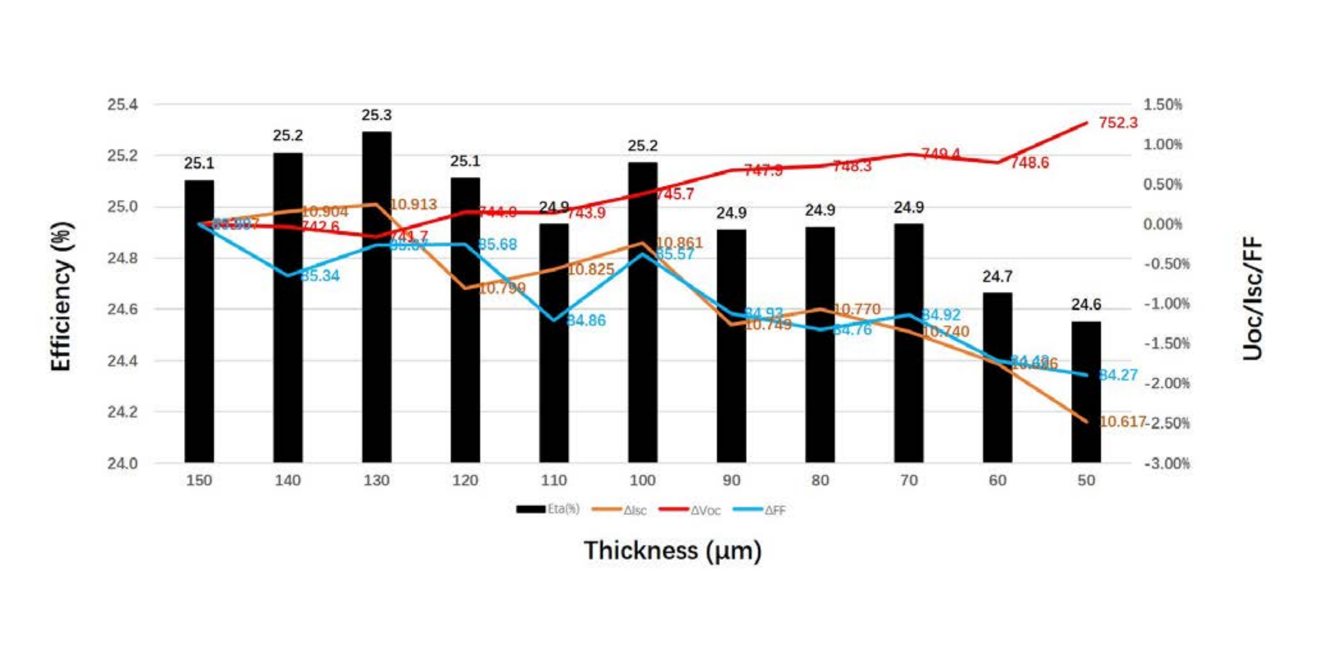


Fig. 2. Electrical characteristics of HJT 2.0 with different thicknesses

New module technologies

Module technology plays an essential role in the power generation and stability of the final product. In recent years, more and more advanced materials have been utilised for module encapsulation, resulting in high efficiency and high stability of HJT modules, water resistance having long been one of the most significant qualities of encapsulants. As an adhesive, transparent butyl adhesive guarantees not only superb light transmission but also excellent air and water tightness. It can greatly improve the weatherability of the module and effectively extend the product's life. Ultraviolet (UV) degradation has been a significant cause of crystalline silicon solar cell and module degradation.[14] UV light can be transmitted effectively over highly transparent film because it transmits light of different wavelengths well. This causes UV damage to the cells. Typically, the UV cut-off encapsulant film is used to restrict the irradiation of short-wavelength light and thus inhibit UV degradation.[15] Nevertheless, in the technology routes of HJT 2.0 and HJT 3.0, the n-μc-SiOx:H film on the front side is more favourable for short-wave light transmission than the n-a-Si:H film in HJT 1.0. So, the utilisation of UV cut-off film significantly reduces the short-wave response benefits of HJT 2.0 and HJT 3.0. To address this issue, UV conversion encapsulant film can be used as an encapsulant. UV conversion encapsulant film converts the short-wave light (about 300~400 nm) to a slightly longer wavelength band (about 400~500 nm), so that the near-UV light can be absorbed without inhibition, thereby maximising the benefits of n-μc-SiOx:H film. The quantum efficiency (QE) curves demonstrate that the module's response to short-wave light can be effectively improved by employing UV conversion encapsulant film, as shown in Fig. 3.

The UV results (as shown in Fig. 4) indicate that UV conversion encapsulant film provides the HJT 2.0-based modules with excellent resistance to UV degradation.

The development level of HJT in China

HJT 1.0 is now being produced at a mature level in China, with consistent efficiency and yield. The current capacity of the major HJT producers is shown in Table 2. Other companies also have their own pilot test lines in addition to these. Among these production lines, the HJT 1.0 lines were all constructed early on with limited capacity. HJT 1.0 can be updated to HJT 2.0 with a small modification. The majority of HJT producers started HJT 2.0 mass production during 2022, with the result that HJT 2.0 now makes up a greater percentage of total HJT production capacity than HJT 1.0. The primary technologies in the future are HJT 2.0 and HJT 3.0, and large-size and thin wafer technologies will be gradually implemented. New technologies, including high mesh count screen plates, silver-coated copper paste and UV conversion encapsulant film, will be implemented one at a time to further cut costs after confirmation of stability.

To demonstrate the production status in further detail, the following takes Huasun as an example. Huasun completed a 500 MW HJT production line in 2021 with the technical route of HJT 1.0. The products consisted of cells and modules. The cell size was 166*166 mm and the average efficiency in mass production was 24.5%. In 2021, the company carried out its plans for increasing production capacity. As shown in Fig. 5, the daily production capacity of cells reached 187,900 units in June 2021 and full production capacity was achieved by mid-June. The stability of production

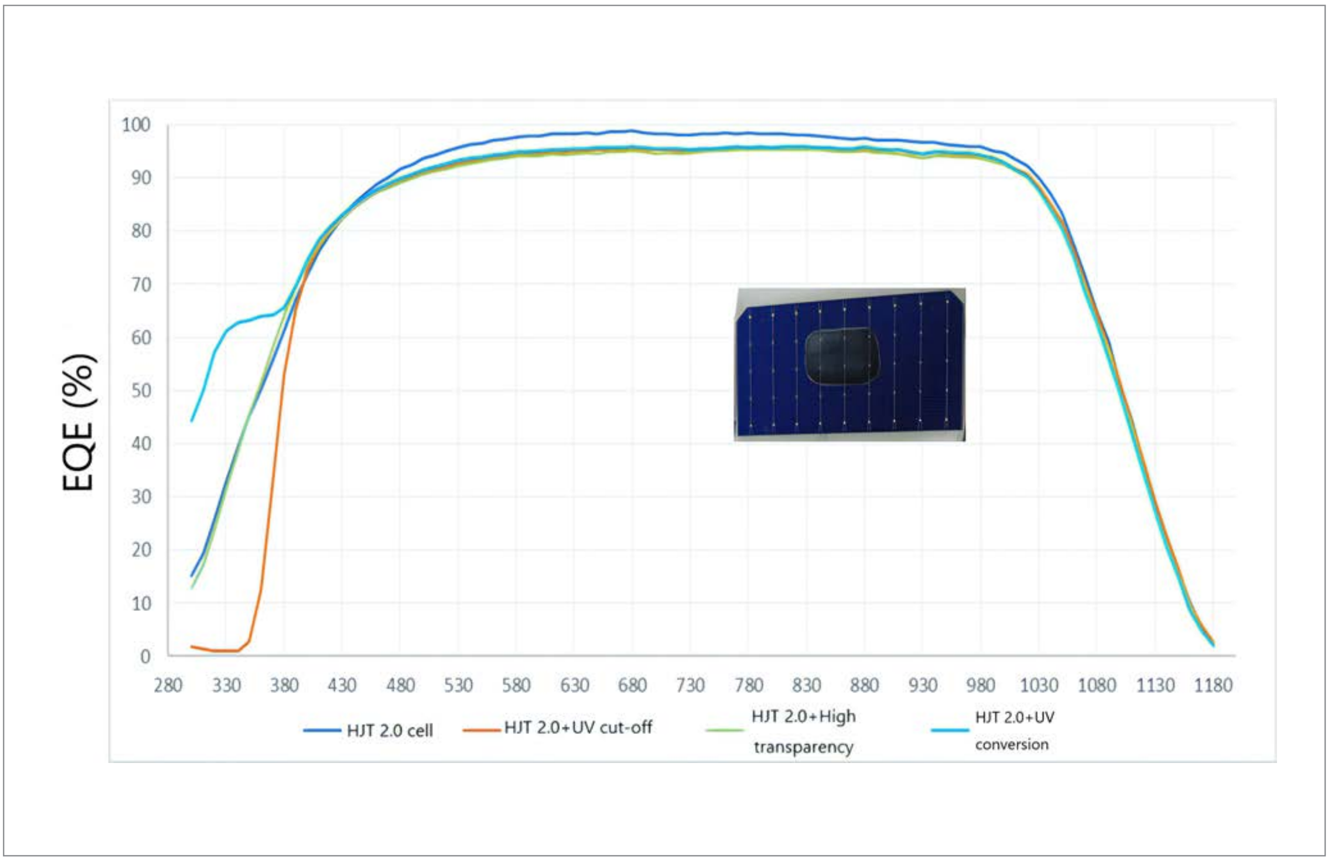


Fig. 3. QE curves of different package films based on HJT 2.0

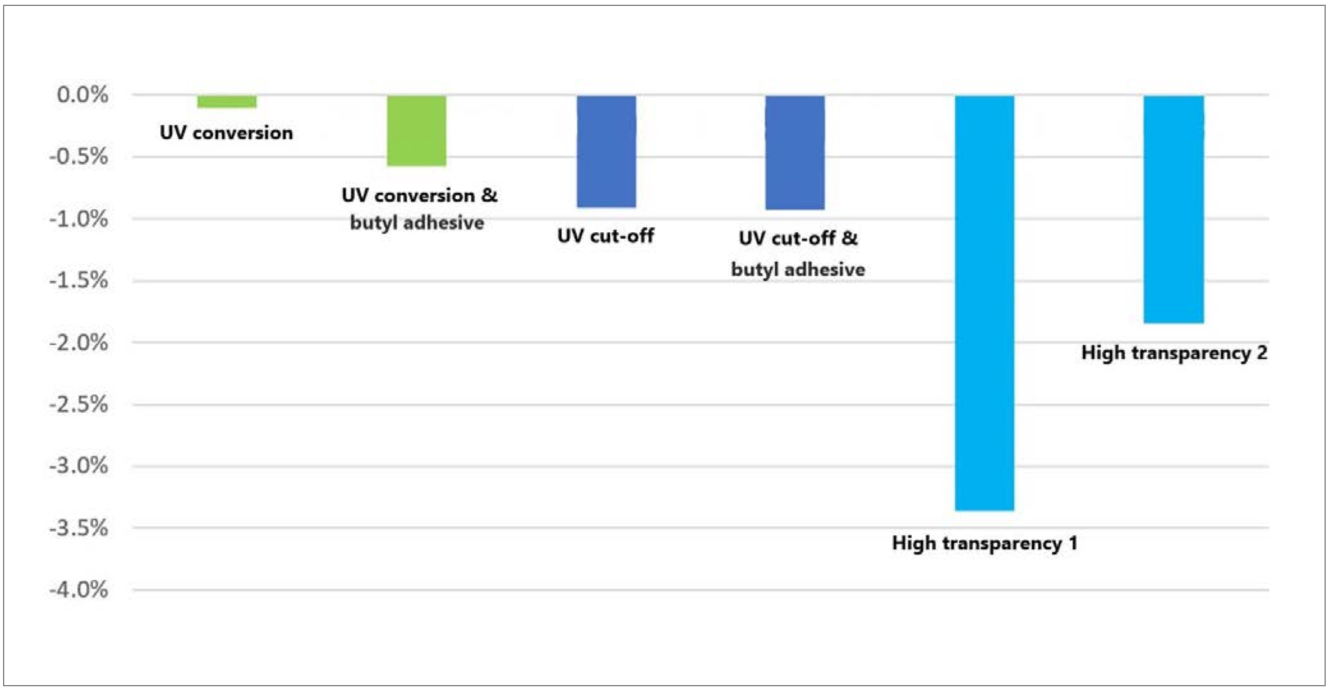


Fig. 4. Outdoor UV experiment for different encapsulant films with HJT 2.0 modules

line equipment continued to improve, the yield for A0 grade reaching 98% and that for A0+A1+A2 reaching 99.5%, equivalent to PERC. After process improvements, a daily output of 245,000 pieces was achieved on 4 July 2021, surpassing 125% of the designed capacity. The production capacity reached the same level of 660 MW in the fourth quarter of 2021.

In 2022, Huasun completed an HJT production line for cells and modules with a capacity of 2GW. The technical route was HJT 2.0 and capacity is currently climbing. Unlike the 500MW production line, this line produces 210*210 mm half-cells. In addition, this production line involves a phosphorous diffusion gettering process to remove impurities from the n-type silicon wafers, to further improve the

Company	Established HJT 1.0 (MW)	Established HJT 2.0 (MW)	Planning (MW)
Huasun	500	2,200	17,500
Company T	1,000	250 (upgrading from 1.0 to 2.0)	
Company J		1,200	4,800

Table 2. The capacity of major HJT production companies

efficiency of the cell. The average efficiency in mass production has now reached 24.7%, with maximum efficiency at 25.21%, as shown in Fig. 6. However, there is still room for further improvement.

With the completion of the 500 MW production line in 2021, the Huasun R&D Centre began building a laboratory to conduct in-depth research on HJT 2.0 and HJT 3.0 technologies. In May 2021, Huasun collaborated with Maxwell to set a world-record HJT efficiency of 25.26%. Self-developed HJT 2.0 technology was launched after completion of the 2GW production line in April 2022, and will be upgraded to increase capacity and efficiency. Simultaneously, the R&D Centre is also actively researching into HJT 3.0 technology. Under the same equipment conditions as the production line, a maximum efficiency of 25.6% was achieved in August 2022 (validated by the Chinese Institute of Metrology) while, at the same time, many of the stability issues that could affect the final efficiency were resolved. As a consequence, the foundation was laid for the industrialization of HJT 3.0.

Summary and expectation

HJT technology has progressed as expected. By combining a variety of modern photovoltaic technologies, it has increased efficiency and decreased cost.

In the future, HJT 3.0 will become the mainstream, achieving a levelised cost of electricity (LCOE) comparable to products of other technology lines, like PERC. Huasun has been at the forefront of this technology since its inception, pioneering the development of HJT, and will continue to expand its production capacity to achieve mass production of HJT 3.0. Combined with thin wafer technology, new metallization technologies and new module technologies with different encapsulant materials, Huasun will further reduce costs and improve the efficiency of mass-produced cells and modules, making HJT the most cost-effective photovoltaic technology. The Huasun R&D Centre will carry out additional research into new HJT structures, focusing on heterojunction back contact (HBC) and tandem cells, while the company gradually implements R&D outcomes into its production lines.

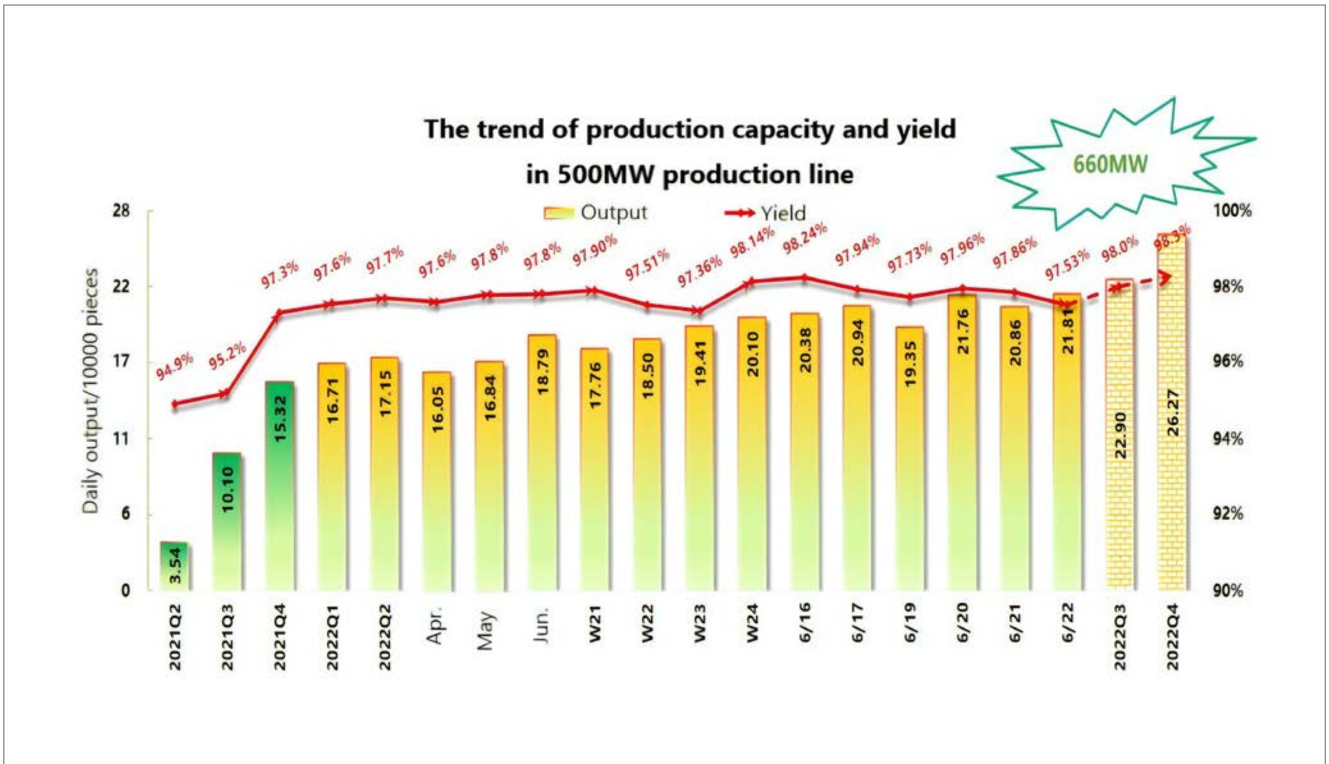
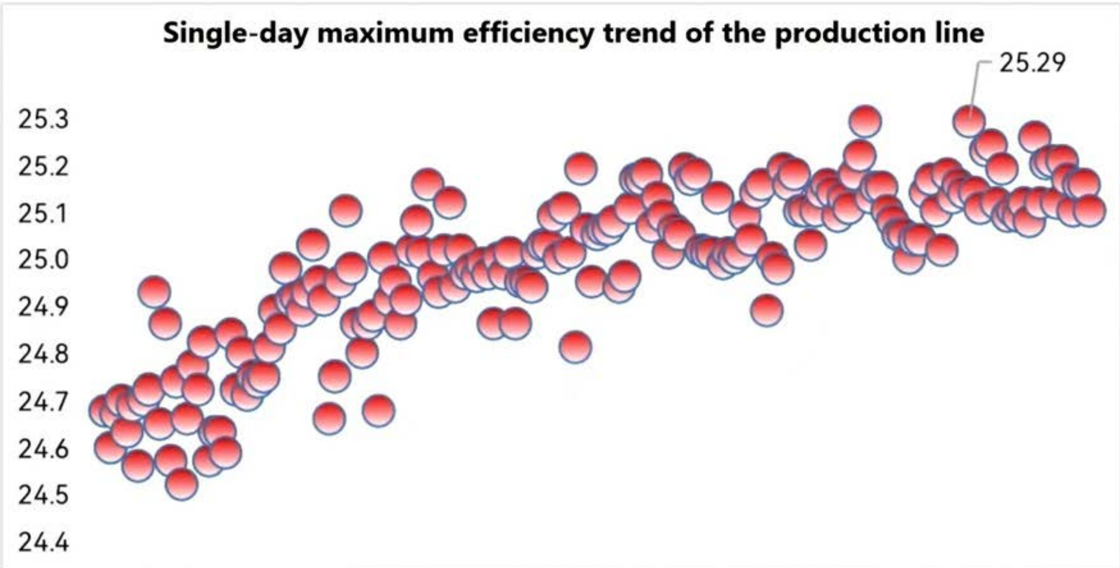


Fig. 5. Production status at Huasun in 2021



Qua	Eta_Ave	Eta_Max	Uoc	Jsc	FF	Pmpp	Rser	Rshunt
5467	24.92	25.21	0.746	39.19	85.24	5.49	0.0047	1458.69

Fig. 6. Maximum efficiency trend of 2 GW production line at Huasun (Qua = quantity, Eta_Ave = average efficiency, Eta_Max = maximum efficiency, J_{sc} = short-circuit current density, P_{mpp} = power at maximum power point, R_{ser} = serial resistance, R_{shunt} = shunt resistance)

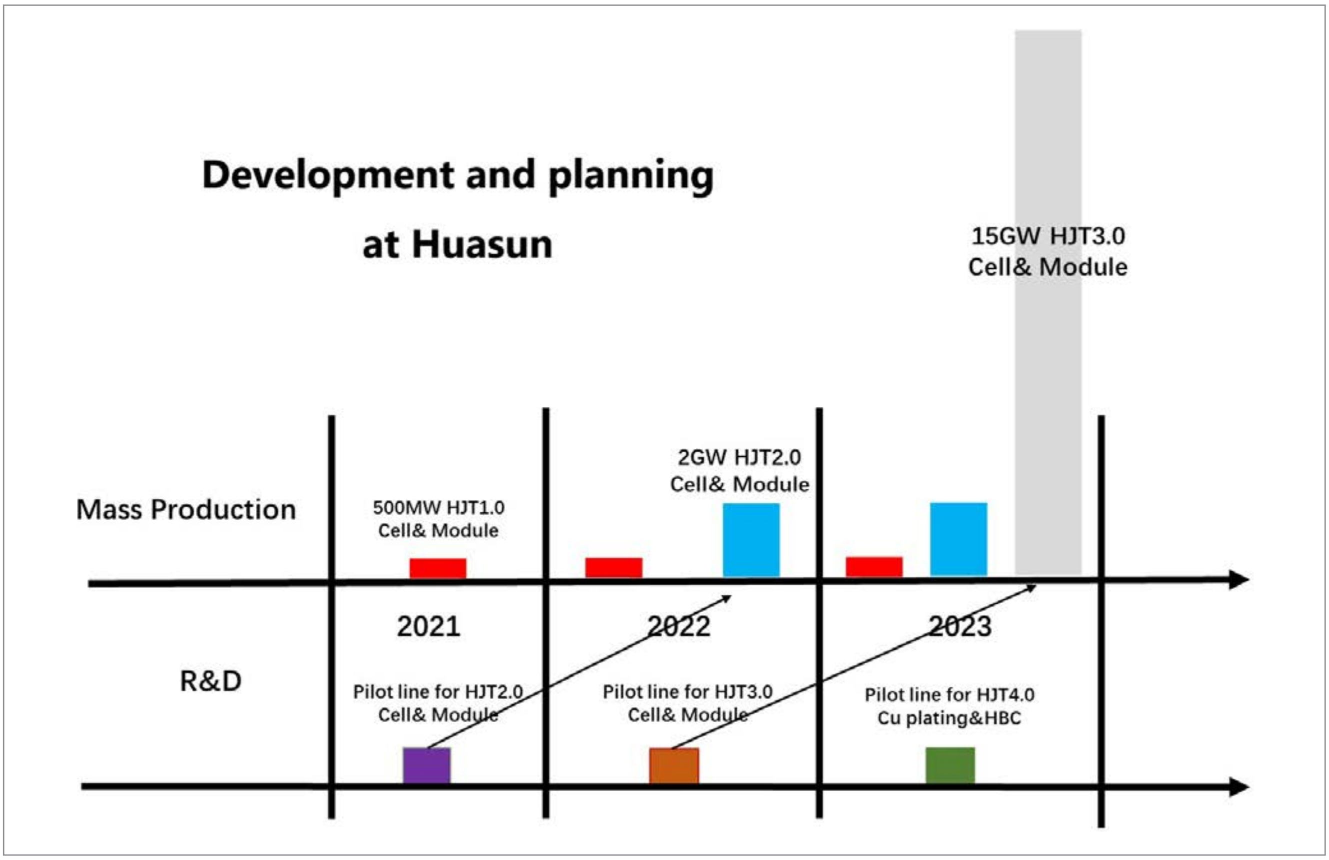


Fig. 7. Development and planning for HJT at Huasun

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Towards high-efficiency POLO IBC solar cells based on a PERC+ processing technology

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Abstract

We develop a novel manufacturing process sequence for polysilicon on oxide (POLO) IBC solar cells by applying a local PECVD SiOxNy/n-a-Si deposition through a glass shadow mask to form the structured carrier-selective n-poly-Si emitter in a single process step. The other POLO IBC processing steps such as AlOx/SiN surface passivation, laser contact opening and Ag and Al screen printing are very similar to those of today's bifacial PERC+ cells, thereby targeting a very cost-competitive manufacturing process. POLO IBC precursors without metal contacts exhibit an excellent implied Voc (iVoc) of 741 mV. The first fully processed POLO IBC cells on M2-sized Ga-doped Cz wafers achieve conversion efficiencies of up to 23.0% with Voc = 708 mV, Jsc = 41.2 mA/cm2 and FF = 78.7%. The 33 mV difference between iVoc and Voc is caused by additional Jo contributions of the Ag and Al metal contacts, which we will improve in the future. These initial results have been obtained by applying a lab-type PECVD tool for the SiOxNy/n-a-Si deposition through shadow masks. Afterwards, we transfer the process to a mass-production c.plasma PECVD tool from centrotherm, which is installed at the ISFH SolarTeC, delivering very promising results also outlined in this paper. As next steps towards production readiness, we aim at further increasing the POLO IBC conversion efficiency towards 25% and implementing an automated shadow mask loading into the industrial c.plasma tool.

Introduction

The global photovoltaics market today is still mostly based on monofacial PERC or bifacial PERC+ solar cells [1]. In mass production, PERC and PERC+ cells achieve conversion efficiencies of around 23% by applying a best-in-class and cost-effective manufacturing process [1]. Nevertheless, the carrier recombination in the phosphorus-doped emitter and at the Ag front contacts limits the Voc and efficiency potential of PERC+ cells to below 700 mV and 24%, respectively [2].

Applying a new model for carrier selectivity [3], ISFH developed the POLO IBC cell [3,4] as next-generation cell technology. The POLO IBC cell design builds on today's industrial PERC+ cells by continuing to use Ga-doped Cz wafers, an AlOx/SiNy rear passivation and Al finger base contacts. However, it replaces the efficiency-limiting phosphorus emitter with a carrier-selective POLO [3,5] contact on the rear side, thereby drastically increasing the Voc potential up to 733 mV with an efficiency potential of up to 25.5%, as confirmed by Quokka simulations [6]. As process technology for POLO IBC cells, ISFH developed a PECVD SiO_xN_y/n-a-Si deposition process for the POLO stack using a lab-type tool with N2O in-situ plasma oxidation, resulting in an excellent passivation quality after firing with J_o = 2 fA/cm² [7]. Glass-based shadow masks enable the confined local PECVD deposition of the SiON/n-a-Si layer stack onto the silicon wafer [8], thereby facilitating a very lean POLO IBC process sequence, as proposed in [9,10].

"The POLO IBC cell design builds on today's industrial PERC+ cells...."

This paper is an abridged version of a recent conference contribution [11], where we report the first fully processed POLO IBC cells, based on local PECVD SiO_xN_y/n-a-Si deposition through a shadow mask, applying a lab-type single-wafer as well as a mass-production type PECVD tool, yielding conversion efficiencies of up to 23.0%. Our cost calculations demonstrate that POLO IBC cells manufactured with this process can be cost-competitive against today's mainstream PERC+ cells.

PECVD SiOxNy/n-a-Si process development and transfer

We have developed a PECVD process to deposit the SiO_xN_y/n-a-Si layer stack in-situ in one deposition process, as published in [7], using a lab-type single wafer tool (Clustertool, Von Ardenne). The lab PECVD tool applies a capacity-coupled plasma source, an in-situ plasma oxidation using N2O to grow an approximately 1.7 nm-thin SiO_xN_y, and SiH4, PH3 and H2 to deposit a 120 nm-thick in-situ-doped n-a-Si layer. To assess the passivation quality, symmetrical n-type Cz test wafers are processed with the PECVD SiO_xN_y/n-a-Si, followed by annealing in N2 at 850°C, PECVD deposition of a 100-nm thick SiNx layer and firing

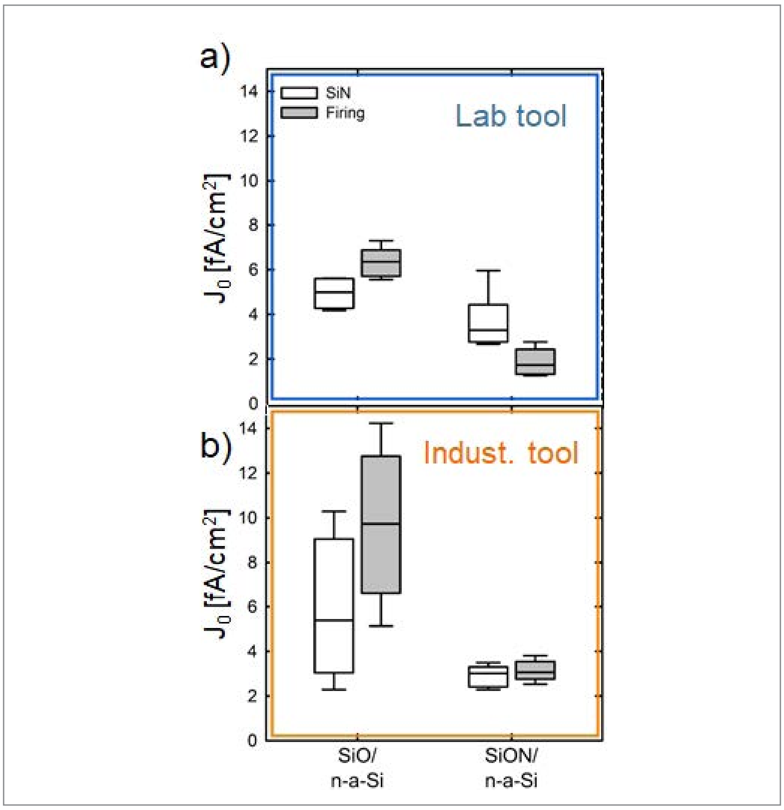


Figure 1: Saturation current density J_0 of symmetrical test wafers passivated with either SiOx/n-a-Si or SiO_xN_y/n-a-Si. Both a) the lab PECVD tool and b) the industrial PECVD tool achieve excellent J_0 values after firing of 2 and 3 fA/cm², respectively, when applying the interfacial SiO_xN_y. In contrast, when using an SiO_x either by a) thermal oxidation or b) plasma oxidation, the surface passivation degrades after firing to J_0 values of 6 and 10 fA/cm², respectively.

at 810°C. Figure 1 a) shows the results obtained with the lab tool, as published in [7], where the SiO_xN_y interface exhibits excellent firing stability in contrast to a thermal SiOx interface, which slightly degrades during firing.

After adapting, implementing and optimising the PECVD SiO_xN_y/n-a-Si recipe to an industrial c.plasma tool from centrotherm at the ISFH SolarTeC (see Figure 2), this tool also achieves very good J_0 values of 3 fA/cm² after firing, as displayed in Figure 1 b). For comparison, we develop an in-situ plasma oxidation using O2 at the industrial tool. As shown in Figure 1 b), the PECVD SiOx/n-a-Si layer stack exhibits higher J_0 values of 6 fA/cm² after SiN deposition, which degrade to 10 fA/cm² after firing. Hence, for both tools, the SiO_xN_y interface grown by in-situ N2O plasma oxidation delivers the best J_0 values after firing. A TEM study confirms that the N2O plasma oxidation incorporates nitrogen at the c-Si / SiO_xN_y interface [11]. It has been shown for SiN layers that nitrogen increases the silicon-to-hydrogen bonding energy, thereby reducing the hydrogen outdiffusion during firing [12]. Similarly, nitrogen at the c-Si / SiO_xN_y interface could increase the hydrogen bonding energy to silicon bonds, thereby contributing to the improved firing stability demonstrated in Figures 1 a) and b).

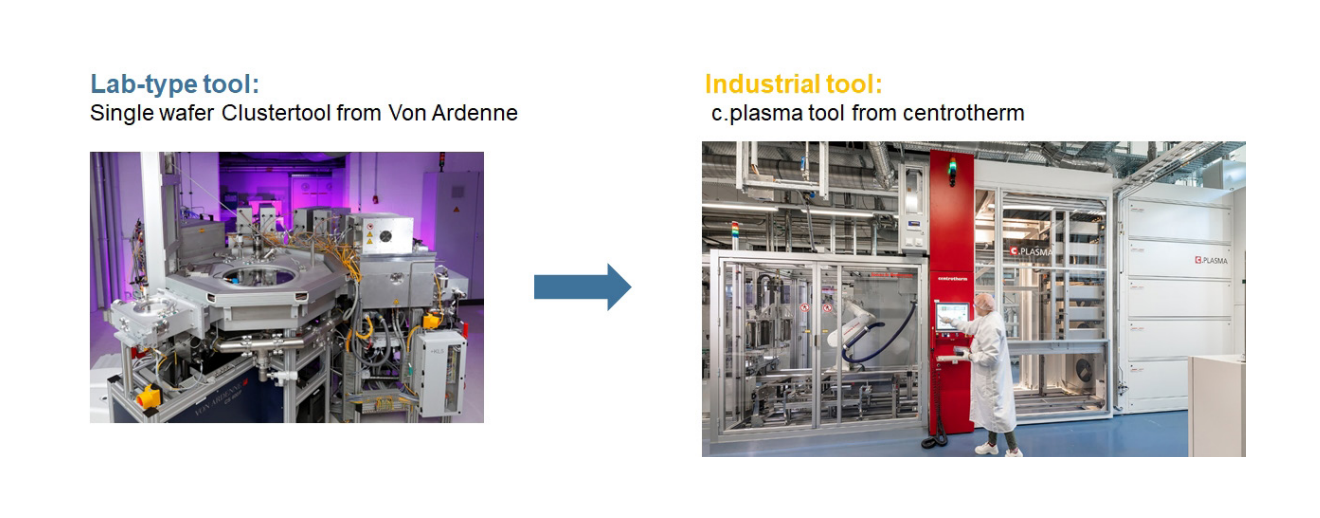


Figure 2: Development of the in-situ PECVD deposition of the $SiOxN_y$/n-a-Si layer stack began with the lab-type tool (left image). After initial promising results, we transferred and adopted the PECVD $SiOxN_y$/n-a-Si recipe to the industrial c.plasma tool at the ISFH SolarTeC (right image).

POLO IBC cells with shadow masks

3.1 Process sequence with shadow masks

The POLO IBC process flow applying the local PECVD SiO_xN_y/n-a-Si deposition through a glass shadow mask is shown schematically in Figure 3. At the beginning, 1Ωcm Ga-doped M2-sized Cz wafers are textured on both sides and subsequently polished on the rear side according to step 1 in Figure 3. Afterwards, we locally deposit the SiO_xN_y SiO_xN_y/n-a-Si layer stack through a glass shadow mask provided by LPKF, by using either the lab-type PECVD tool or the industrial PECVD tool. Step 2 in Figure 3 is completed by annealing the wafers in a nitrogen atmosphere at 850°C. Both sides of the wafer are passivated by an AlOx/SiN layer stack (step 3), followed by laser contact opening (LCO) of the AlOx/SiN at the rear-side base region (step 4). Finally, the Al contacts are screen-printed on top of the LCOs and the Ag contacts are printed aligned to the n-poly-Si. The process sequence is completed by firing the wafers at around 810°C, where the Al contacts locally alloy with the silicon wafer forming an Al-BSF and the Ag paste dissolves the AlOx/SiN layer contacting the n-poly-Si. Compared to an industrial PERC+ process, this POLO IBC process uses the same steps of texturing, rear polishing, AlOx/SiN deposition, LCO, and screen-printing of Al and Ag pastes. Only the POCl3 diffusion and laser doping is replaced by the local PECVD SiO_xN_y/n-a-Si deposition; see also the step-by-step process flow comparison in the cost calculation displayed in Figure 7.

A photograph of an M2-sized glass shadow mask in front of a Cz wafer, which received the local SiO_xN_y/n-a-Si deposition, is displayed in Figure 4 a). A close-up image by light microscopy in Figure 4 b) reveals that the local SiO_xN_y/n-a-Si layer width matches the shadow mask layout within an accuracy of ± 10 µm. Figure 4 c) displays a light microscope image of the rear side of a fully processed POLO IBC cell including screen-printed Al and Ag fingers, which are well aligned to the local SiO_xN_y/n-a-Si layers within an accuracy of ± 20 µm.

"...the SiOx Ny interface exhibits excellent firing stability..."

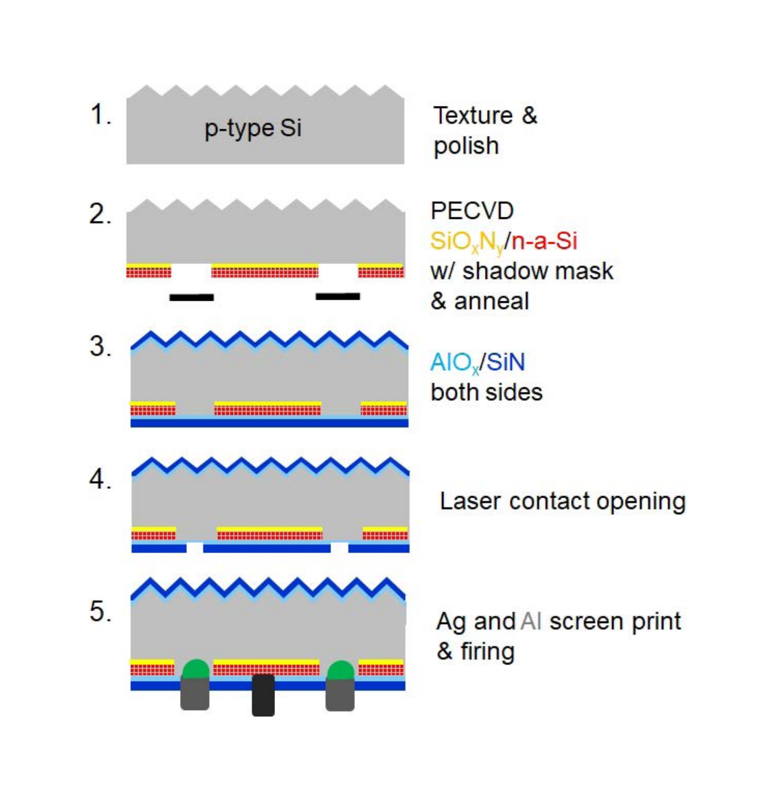


Figure 3: Schematic drawings of the lean POLO IBC process flow applying the local PECVD SiO_xN_y/n-a-Si deposition through a glass shadow mask. All other processing steps are very similar to today's PERC+ solar cell technology.

3.2 Implied Voc results of POLO IBC precursors without metal contacts

We process implied Voc (iVoc) precursors according to the process flow in Figure 3 up to step 3, in order to assess the Voc potential of the POLO IBC cells. We skip LCOs (step 4) and screen-printing (step 5), but apply firing to the iVoc precursors. When depositing the local PECVD SiO_xN_y/n-a-Si layer in the lab-type tool, we obtain excellent average iVoc values of 741 mV determined by infrared lifetime mapping (ILM), as shown in Figure 5. This high iVoc corresponds to a total J_o of 10 fA/cm² of the POLO IBC precursor, revealing the excellent passivation qualities of the local SiO_xN_y/n-a-Si and AlO_x/SiN layers, as well as a very low $J_{o,}$bulk of the Ga wafer, which is in accordance with the simulations in [7]. Applying the industrial PECVD tool for the local SiO_xN_y/n-a-Si deposition, we obtain average iVoc values of 721 mV, as shown in Figure 5. However, these wafers have not yet received the optimised PECVD SiO_xN_y/n-a-Si recipe in Figure 1 b), but a previous recipe exhibiting higher J_o values. When applying the improved recipe of Figure 1 b), we expect that the iVoc values of POLO IBC precursors processed in the industrial tool will approach the high iVoc values obtained with the lab-type tool.

3.3 POLO IBC cell results using shadow masks

First, we have processed POLO IBC cells in two subsequent batches using the lab-type PECVD tool as well as a first cell batch using the industrial PECVD tool. The cells are measured with an IV tester (LOANA from pv tools) at ISFH, which uses contact bars to contact the busbars at full length at the rear side of the cells and includes sense pins to measure the voltage of the cell. The illumination is calibrated using the internal calibration of the IV tester, since we do not yet have a POLO IBC cell measured at a certified calibration lab.

The efficiency of IV parameters, open circuit voltage (Voc), short circuit current (J_{sc}) and fill factor (FF) of POLO IBC cells from the second run using the lab-type tool for local PECVD SiO_xN_y/n-a-Si deposition through a shadow mask are displayed in Figure 6. On average, we obtain 22.8% efficiency and Voc = 712 mV. The best POLO IBC cell of this run exhibits a conversion efficiency of 23.0% with Voc= 708 mV, J_{sc} = 41.2 mA/cm² and *FF* = 78.7%. We attribute the 29 mV difference between iVoc = 741 mV (see Figure 5) and Voc = 712 mV to the high Al and Ag contact area fractions of approximately 3% and 10%, respectively. When assuming a typical $J_{o,}$Al-BSF of 500 fA/cm² [2] and J_o,Ag of 150 fA/cm², the full metallisation would account for an area-weighted J_o,met of 30 fA/cm², which explains the delta between the measured Voc and iVoc. By reducing the metal area coverage and by further improving the Ag contact properties, we expect to achieve higher Voc values and higher conversion efficiencies in the near future.

The POLO IBC cells using the industrial PECVD tool were processed in two different split groups. Split group 1 received the full PECVD SiO_xN_y/n-a-Si deposition through the shadow mask. Split group 2 received a wet chemically grown SiOx interface by O3 dissolved in DI water, followed by depositing the PECVD n-a-Si layer through the shadow mask. Figure 6 shows the POLO IBC cell results obtained with split 2 using the wet chemical SiOx interface and the local PECVD n-a-Si. We obtained average efficiencies of 21.8% and Voc values of 710 mV with a best cell efficiency of 22.3%. The split with the full PECVD SiO_xN_y/n-a-Si deposition through the shadow mask is not shown in Figure 6. The resulting Voc and J_{sc} values are very similar but the *FF* is significantly lower, which we attribute to the PECVD SiO_xN_y being too thick. We are currently optimising the SiO_xN_y thickness for the industrial tool and will apply it in combination with the improved PECVD SiO_xN_y/n-a-Si recipe of Figure 1 b) to the next POLO IBC cell run. Thereby, we expect that the conversion efficiencies obtained with the industrial tool will approach the values obtained with the lab tool.

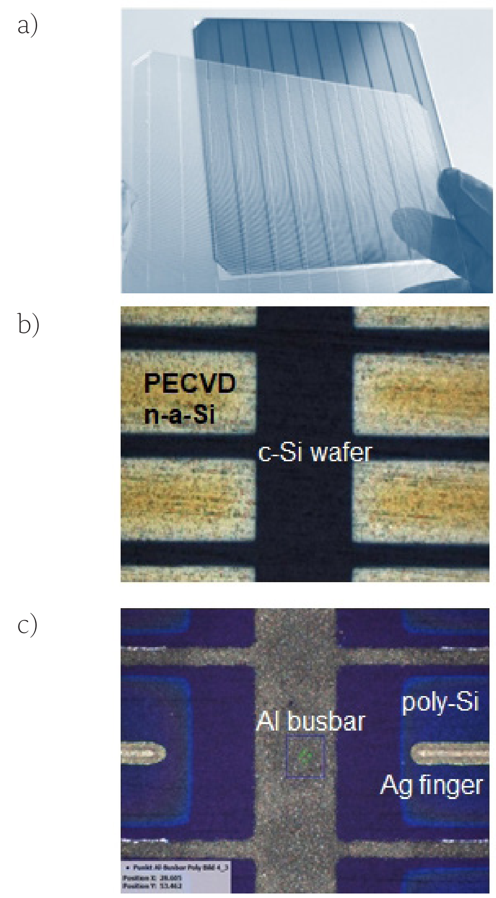


Figure 4: a) Photograph of an M2-sized glass shadow mask in front of a Cz wafer with local SiO_xN_y/n-a-Si layer stack. b) Light microscope image of a local SiO_xN_y/n-a-Si layer stack deposited through the shadow mask in the industrial PECVD tool. c) Light microscope image of the rear side of a fully processed POLO IBC cell including screen-printed Al and Ag fingers, which are well aligned to the local SiO_xN_y/n-a-Si layers.

Cost assessment of POLO IBC solar cells manufactured with shadow masks

Here, we compare the cost of ownership of each cell manufacturing step using a cost model from ISC Konstanz, as shown in Figure 7, in order to assess the future economic competitiveness of POLO IBC cells manufactured with shadow masks versus today's mainstream PERC+ cells. Assuming M6 wafer size, 5 GWp production in EU and Ag paste costs of 700 US$/kg, we calculate the POLO IBC cell processing costs to be 4.6 US$cent/Wp, applying the cost of ownership values per process step as shown in Figure 7 and assuming a POLO IBC cell efficiency of 25%. As a benchmark, 23% efficient PERC+ cells are currently costed very similarly at 4.5 US$cent/Wp. The marginally higher processing costs of POLO IBC originate from the PECVD SiO_xN_y/n-a-Si process, which is more expensive than the POCl3 diffusion used for PERC+. Based on preliminary experimental results, we target that one shadow mask can be used for about 1000 subsequent PECVD depositions and hence only minimally contributes to the PECVD SiO_xN_y/n-a-Si processing costs.

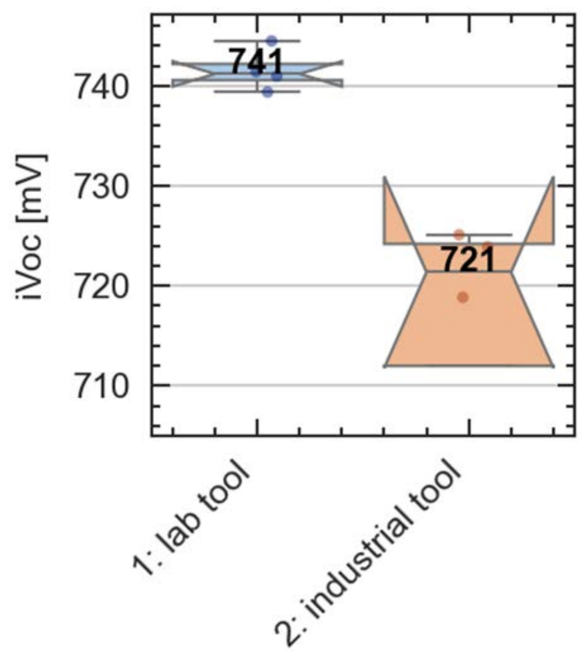
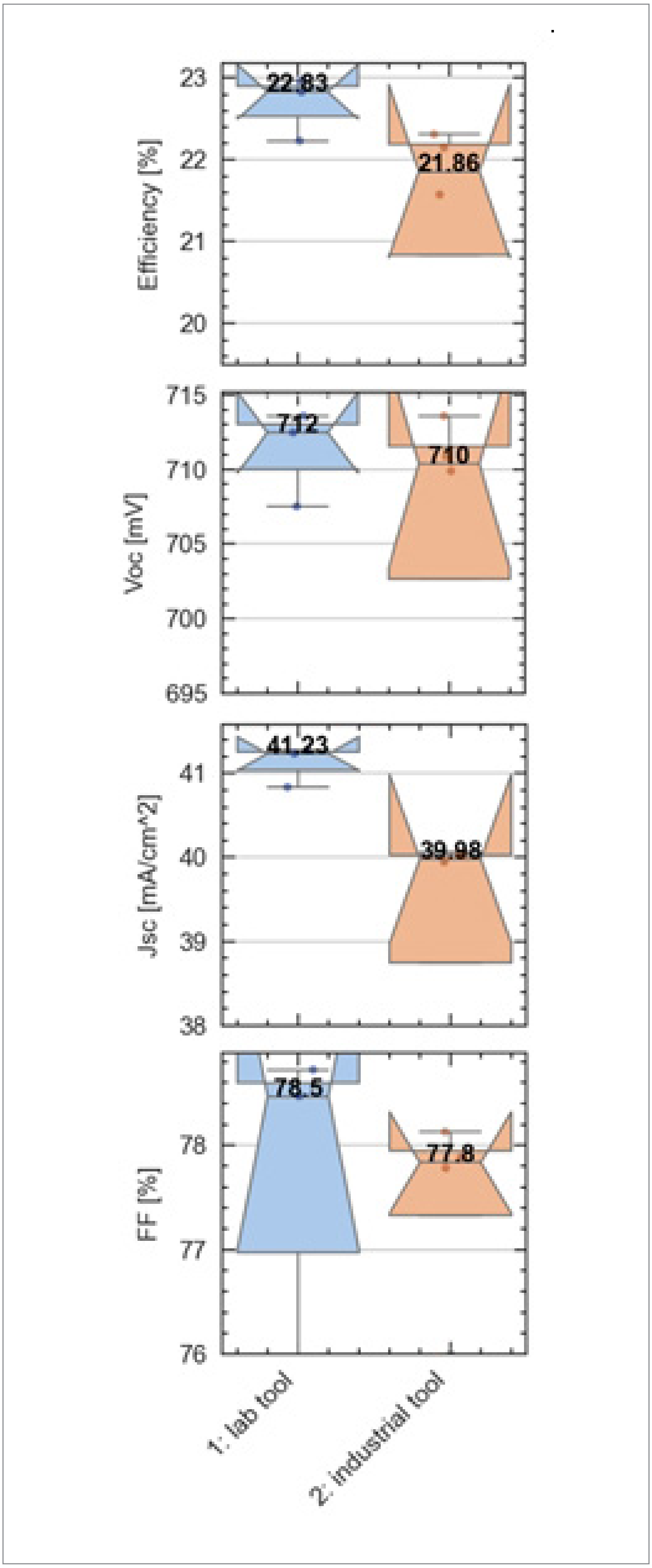


Figure 5: iV_{oc} values of POLO IBC precursors without metal contacts where the local PECVD SiO_xN_y/n-a-Si deposition was performed in the lab tool (group 1) or the industrial tool (group 2).



IV parameters of POLO IBC cells with local PECVD deposition through a shadow mask using either the lab-type or industrial tool.

"…. we expect that the conversion efficiencies obtained with the industrial tool will approach the values obtained with the lab tool"

Using the ISC Konstanz cost model, we calculate that POLO IBC modules will produce electricity in utility-scale (and residential) applications ca. 4% (and ca. 7%) cheaper compared to PERC+ modules, since the 9%rel higher cell efficiency will substantially reduce the area-related balance of system costs per kWp. Hence, this POLO IBC technology is attractive for new cell production lines as well as for upgrading PERC+ fabs to POLO IBC with minimal conversion investment.

Conclusion

In this paper, we demonstrated a novel manufacturing process sequence for POLO IBC solar cells by applying a local PECVD SiO_xN_y/n-a-Si deposition through a glass shadow mask to form the structured carrier-selective n-poly-Si layer in a single process step. After developing the process using a lab-type tool, we transferred the PECVD SiO_xN_y/n-a-Si to an industrial c.plasma tool and obtained an excellent J_0 of 3 fA/cm² after firing. Fully processed POLO IBC solar cells on M2-sized Ga-doped Cz wafers exhibited conversion efficiencies of up to 23.0% with Voc = 708 mV, J_{sc} = 41.2 mA/cm² and *FF* = 78.7% when processed with the lab PECVD tool, alongside an excellent iVoc of 741 mV. We attribute the 33 mV difference between iVoc and Voc to additional J_0 contributions of the Ag and Al metal contacts, which is subject to future improvements. The first POLO IBC solar cells processed with the c.plasma tool with shadow masks achieved conversion efficiencies of up to 22.3% and average Voc values of 710 mV. As next steps towards production readiness, we aim at further increasing the conversion efficiency towards 25% and implementing an automated shadow mask loading into the industrial c.plasma tool.

Acknowledgements

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	PERC+	POLO-IBC
Cell Efficiency	23.00%	25.00%
	USDct/Wp	USDct/Wp
KOH batch texture	0.52	0.48
P-Diffusion	0.27	
Edge isolation and PSG removal SSE	0.56	0.52
PECVD SiON/na-Si with shadow mask		0.40
Anneal /SiO2 or Anneal N2	0.15	0.20
PECVD SiNx/AIOx	0.49	0.45
PECVD SiNx/AIOx/SiNx	0.43	0.45
Laser SiNx ablation	0.09	0.09
Printing 4 Stage (w/o paste cost)	1.12	1.03
pure Ag cost USD/cell	0.88	1.01
Total cell processing cost (w/o wafer)	4.51	4.62

Figure 7: Cost-of-ownership calculations of POLO IBC versus PERC+ cell process costs, applying a cost model from ISC Konstanz. Whereas the cell processing costs are comparable, we expect that the levelized cost of electricity (LCOE) of POLO IBC modules in utility-scale (residential) applications will be up to 4% (7%) cheaper due to the higher conversion efficiency potential.

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Green wafers can lower costs and reduce carbon emissions in manufacturing

Frank Siebke, NexWafe GmbH, Germany

Abstract

While solar photovoltaics (PV) produce no greenhouse gas (GHG) emissions during operation, significant GHG emissions are associated with their production and transportation.
As the world transitions to renewable energy sources and moves to a hydrogen economy, PV have to become greener. Silicon wafers are the most energy-intensive component of a PV module. Conventional wafer production contains several high-temperature processes, such as polysilicon production and ingot pulling. NexWafe offers a cleaner, more efficient and cheaper solution. Our EpiNex™ wafers enable higher efficiencies, lower costs and reduced carbon emissions in wafer manufacturing by more than 70% when compared with the conventional Czochralski process in regions that rely on coal-based electricity. NexWafe's innovative and unique technology creates the opportunity to profitably manufacture ultra-low-carbon green solar wafers.

Introduction

The energy transition and the move towards a green hydrogen economy are motivated by the need to limit global warming. The Intergovernmental Panel on Climate Change (IPCC) has shown that global warming can be stopped if the deployment of renewable energies is accelerated. However, the window of opportunity to achieve the 1.5°C Paris Agreement goal is closing fast.

In its 2021 *World Energy Transitions Outlook*, the International Renewable Energy Agency (IRENA) envisions that solar PV capacity will need to reach more than 14,000 GWp cumulatively by 2050 [1] for the energy transition to be reached. At the same time, the estimated remaining carbon budget from the beginning of 2020 to limit global warming to 1.5°C with a likelihood of 83% is less than 300 Gt CO_2 [2].

This puts a limit on how much CO_2 can be emitted, even while producing renewable energy infrastructure, such as photovoltaic (PV) modules.

Crystalline-silicon-based PV is the dominant technology for the deployment of solar energy today. Impressive cost reductions in silicon-based PV have been achieved by scaling up production over the past two decades. However, the need remains for increased efficiencies, further lowering production costs and reducing the greenhouse gas (GHG) emissions associated with the production of PV modules.

“...is imperative for PV manufacturing to become greener and more efficient.”

Results from modelling by Müller et al. show the potential environmental impacts: solar modules produced in China are linked to emissions of 810 kg CO_2-eq/kWp of which 62.7% can be directly attributed to wafer production [3].

To put this into perspective, producing the required 14,000 GWp of PV modules with conventional technology alone would consume more than 3% of the world's remaining CO_2 budget. In light of this, it is imperative for PV manufacturing to become greener and more efficient.

NexWafe's direct gas-to-wafer technology offers a pathway to reduce the carbon emissions in wafer production by more than 70%, cutting the emissions of module production by half.

Conventional wafer production

Wafers are produced in an energy-intensive process chain. Conventional wafer production is inherently complex and involves the following main energy-intensive and resource-inefficient steps: polysilicon production, crushing, ingot pulling, cropping, squaring, bricking and sawing.

Polycrystalline silicon is the key feedstock in the crystalline-silicon-based PV industry. The so-called Siemens process is the most widespread for the production of polysilicon. In a Siemens reactor, graphite electrodes pass current through a U-shaped silicon core. Trichlorosilane (TCS) and hydrogen are injected into the reactor. At the hot silicon surface, the TCS undergoes hydrogen reduction in a process similar to chemical vapour deposition (CVD) to form solid silicon and gaseous hydrochloric acid. Solid polysilicon deposits onto the silicon seed. After the process is complete, the large rods are broken into chunks or chips of various sizes.

Monocrystalline ingots are typically manufactured via the Czochralski (Cz) process. Polysilicon is melted in a quartz crucible. A seed crystal is dipped into the melt and pulled slowly upwards while being rotated. Since crystal growth occurs at the melt/ingot interface, a cylindrical single-crystal ingot is produced. The silicon grown via the Cz process is characterised by a relatively high oxygen concentration. Another disadvantage of the Cz process is the fact that the dopant distribution is not uniform along the ingot because the segregation coefficient of dopants such as gallium or phosphorus is not unity. This results in a relatively low dopant concentration, hence higher resistivity, at the start of the Cz pulling process and a higher dopant concentration, hence lower resistivity, towards the end of the pulling process.

Following cooling of the finished ingot, its top and tails are removed, and the cylindrical ingot is squared to leave a square or pseudo-square ingot. The squared ingot is then cut into shorter bricks, which are finally sliced into wafers by a wire saw. Wire sawing is an inherently wasteful process due to the unavoidable losses of silicon. Even with today's extremely thin diamond-coated wires, about 30% of the silicon in the bricks is lost.

The EpiNex process – kerfless epitaxial growth of silicon wafers

Various kerfless wafer-manufacturing approaches have been developed to reduce the amount of silicon used. Such kerfless technologies include 1366's direct wafer technology [4], which produces multi-crystalline wafers from the liquid phase, and SiGen's PolyMax technology [5], which separates thin layers from a brick using hydrogen implantation. While some of these approaches have shown the potential to reduce costs, they also compromise the efficiency mainly due to the limitations in the quality of the wafers produced.

In the 1990s, the potential was recognised of epitaxial growth on restructured porous silicon substrates to offer lower manufacturing costs while maintaining or even enhancing solar efficiency. A good overview of the early work on layer-transfer processes for crystalline solar cells is given by Brendel [6]. Since then, several research groups such as ISFH and IMEC worked on improvements of this so-called porous silicon (PSI) process. In 2018, Gemmel et al. grew epitaxial wafers on polished seed wafers, with a resistivity of 3 Ωcm and an

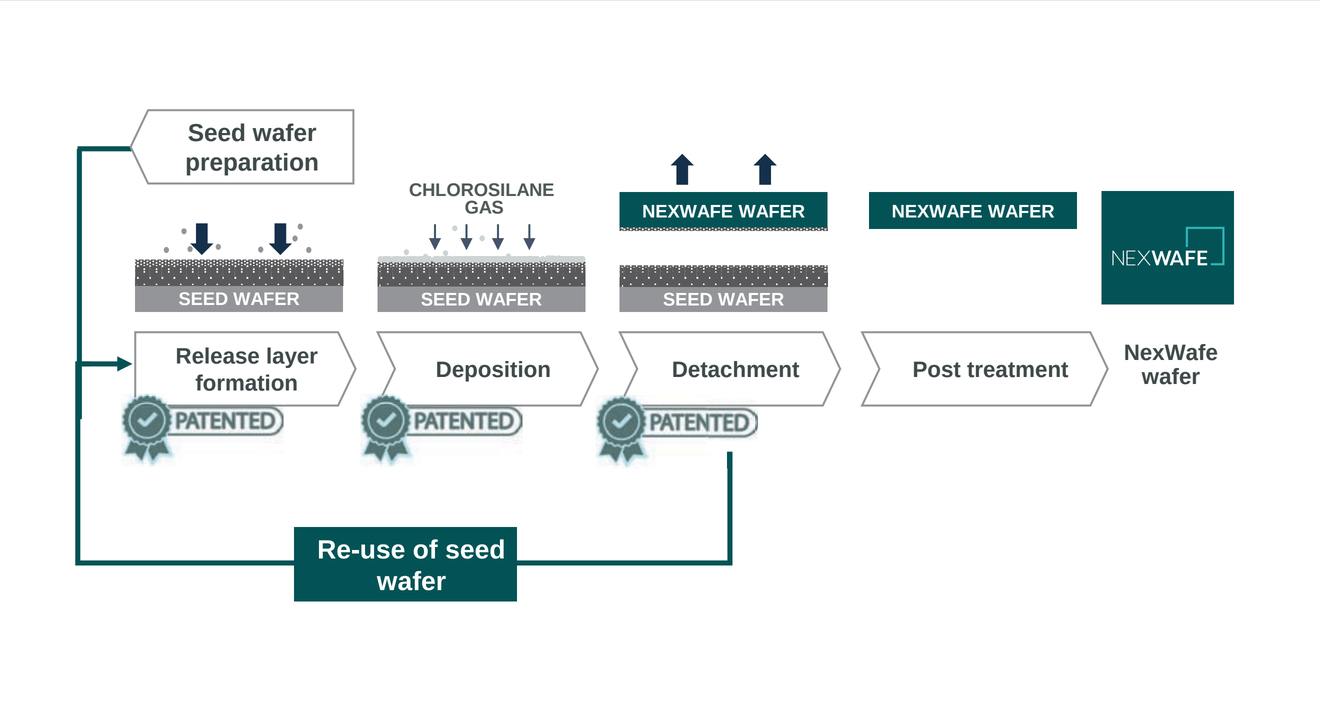

Figure 1: Direct gas-to-wafer process chain

average minority carrier lifetime (MCLT) of 3.2 ms, which could be improved by gettering to very high lifetimes of 4.6–8.0 ms [7]. Solexel and Crystal Solar tried to commercialise a PSI process. In cooperation with IMEC, Crystal Solar demonstrated high solar-cell efficiencies on epitaxially grown wafers but failed to scale-up its technology [8].

NexWafe's direct gas-to-wafer technology (Figure 1) to produce epitaxially grown (EpiNex) wafers is also based on the principles of the PSI process. Unlike earlier attempts, NexWafe's technology builds on processes and equipment that allow high throughput, low cost and large wafer sizes, as demanded by the PV industry.

In the first step, Cz wafers with a resistivity of 10 mΩcm are prepared for use as seed wafers. Chemical mechanical polishing steps, which are common in the semiconductor industry to create 'epi-ready' wafers, are prohibitive in the solar industry because of the associated high cost. Instead of using epi-ready wafers, NexWafe buys Cz wafers and cuts and etches them using a wet chemical etching tool. This tool was designed for solar-cell production to eliminate saw damage and create a surface suitable for the subsequent release layer formation and the epitaxial growth of high-quality EpiNex™ wafers.

Using a proprietary equipment design suitable for high throughput, anodic oxidation is used to create a few microns-thin porous silicon layers on one surface of the seed wafer. Good homogeneity of the porous layers across the total wafer surface is essential. At the same time, a stack of low porosity and high porosity layers is created to enable good detachability and high quality of the EpiNex™ wafer. Figure 2 shows a porous layer stack with a low porosity layer (LPL) at the surface and a high porosity layer (HPL) below the LPL.

Subsequently, the porosified seed wafers are transferred to the epitaxy reactor. During heating to the deposition temperature of over 1100°C, the porous structure reorganises. The pores at the surface of the LPL close and a monocrystalline layer is formed, which then acts as a template for the epitaxial growth. At the same time, the voids of the HPL grow and it transforms into a microscopic cathedral – a large, open space where the roof is supported by a few thin columns.

After reorganisation of the porous layers, the wafers are transferred into the deposition chamber. At temperatures of about 1100°C, silicon is grown by atmospheric pressure chemical vapour deposition (APCVD) from a mixture of chlorosilane and hydrogen. Phosphine or diborane can be used as dopants to grow either n-type or p-type wafers.

The epitaxially grown wafers are mechanically detached from the seed wafers. After the excess silicon, which has grown over the edges of the seed wafer, is removed by grinding or laser scribing, the sandwich consisting of the seed wafer and the EpiWafer is taken by a vacuum gripper and placed on a second vacuum chuck. After applying a vacuum to both sides of the sandwich, the EpiWafer is detached from the seed wafer by applying mechanical stress. The process has been integrated into a fully automated tool, which performs the wafer handling, positioning and detachment.

After detachment, both the seed wafer and the EpiWafer are chemically cleaned to remove the residues of the release layer. A phosphorus-diffusion for gettering, which is a well-known treatment to increase the effective lifetime by reducing extrinsic minority carrier recombination, is applied to the EpiWafer [9]. The seed wafer is reused.

EpiWafer properties

Oxygen content

Oxygen impurities in Cz silicon wafers arise from the dissolution of the quartz crucible used during ingot pulling. Boron-oxygen complexes cause light-induced degradation of solar cells. The PV industry has mitigated this problem by moving towards more expensive gallium-doped wafers. Oxygen creates various kinds of defects in silicon crystals, which can reduce MCLT and thereby reduce cell efficiency [10]. The EpiNex process produces EpiWafers with a lower oxygen concentration of more than an order of magnitude than that of Cz wafers (Figure 3).

NexWafe believes that the low oxygen content inherent to the EpiNex process can enable significant cell efficiency gains versus conventional Cz wafers.

Minority carrier lifetime

The MCLT of a wafer is an important aspect for the electronic quality of a wafer. The MCLT is determined by the quasi steady-state photoconductance (QSSPC) technique [11]. Conventional n-type Cz wafers for solar-cell production are specified to have an MCLT exceeding 1ms for resistivities of 1–7 Ωcm [12]. EpiWafers produced by the EpiNex process meet the industry standards (see Figure 4).

Resistivity control

As discussed in Section 2, doping levels and therefore resistivity vary from one end of an ingot to the other. The resistivity can be seven times lower at the top end than the tail end for n-type ingots [13]. Wafers from the top of the ingot exhibit low doping, high resistivity and high MCLT. Cells fabricated from such wafers exhibit relatively high open-circuit voltage (VOC) but low fill factor (FF). Wafers from the bottom of the ingot provide high doping, low resistivity and low MCLT, and typically exhibit a lower VOC but higher FF. In addition, the longer the crucible is used, the more impurities tend to accumulate in the melt, which will result in a lower MCLT and lower cell efficiencies.

In contrast, the EpiNex process produces wafers doped by adding dopants to the gas phase. The doping level can thus be controlled very accurately by mass flow controllers. As a result, EpiWafers exhibit a very narrow resistivity distribution (Figure 5).

A narrow resistivity distribution allows all wafers to be processed in as close to optimal conditions as possible. Increased average cell efficiency from the cell-manufacturing line and a narrow distribution of cell efficiencies can be achieved.

As discussed, the doping gradient along the length of a Cz ingot is a problem, but the creation of doping gradients within a wafer (i.e. from the surfaces of the wafer to the bulk of the wafer) can be an advantage. Such doping gradients could result in reducing the recombination of carriers in the bulk while maintaining good contact properties. Doping gradients within the wafer could also increase cell efficiency. However, such gradients cannot be produced in conventional wafer manufacturing, but they can be created during the EpiNex manufacturing process simply by changing the dopant concentration during the deposition process. Doping from the gas phase allows a high level of control of the doping level.

"...the EpiNex process can enable significant cell efficiency gains versus conventional Cz wafers."

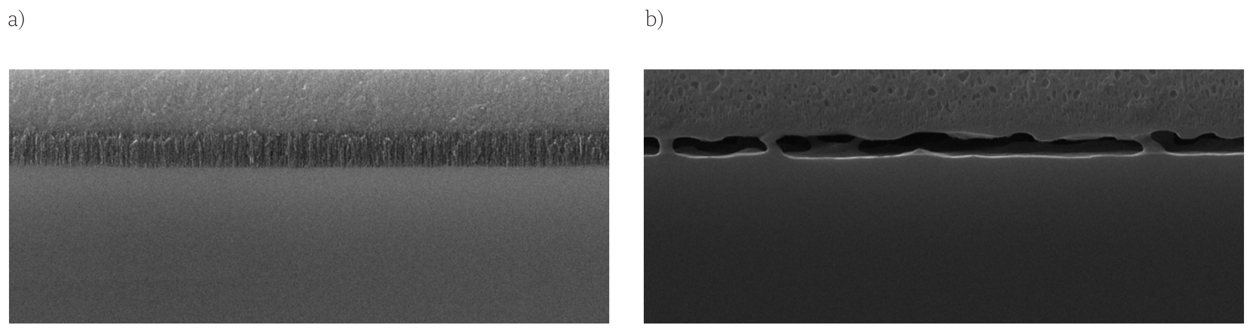

Figure 2: Porous silicon stack (a) after anodic oxidation and (b) after reorganisation

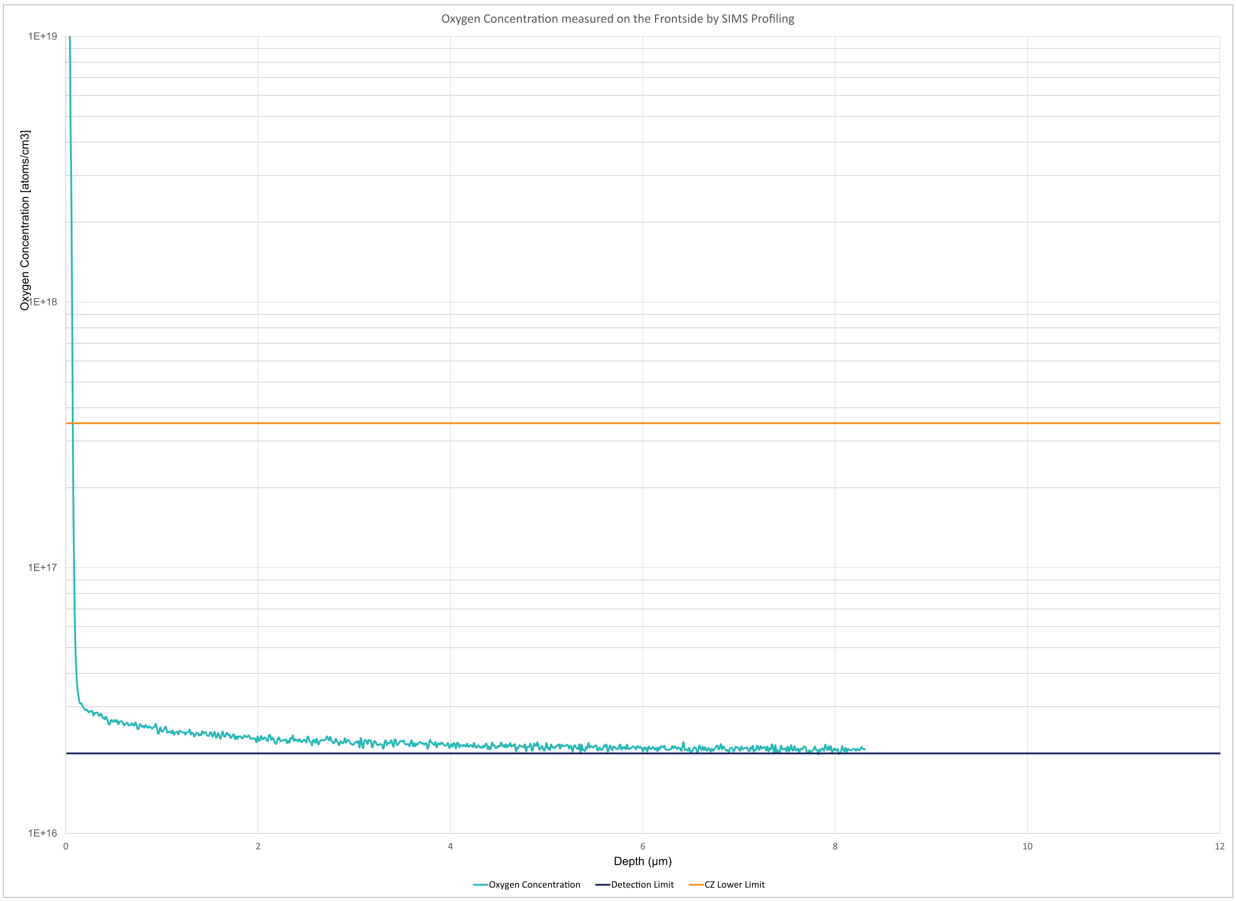

Figure 3: Oxygen concentrations of EpiWafer and Cz wafers

Wafer size

During recent years, PV-wafer manufacturing has been moving towards larger wafer formats. The previously dominant M2 has been replaced by larger formats such as M6 (pseudo-square, 166 mm side length), which are now being phased out as the major PV companies move towards the larger M10 (pseudo-square, 182 mm side length) and G12 (full-square, 210 mm side length) wafer formats. As wafer size increases, the risk of lower manufacturing yields also increases. Yield rates are reported to be lower for G12 in the wafering process, which is an issue that may be amplified by any transition towards thinner wafers or even larger wafer formats. At the ingot level, pull speeds for G12 ingots are reportedly around 20–25% slower than for M6 or M10 ingots, resulting in increased costs. In addition, the G12 format is full-square. Large wings are cut off in the squaring process, which can be recycled but they reduce the energy efficiency of the manufacturing.

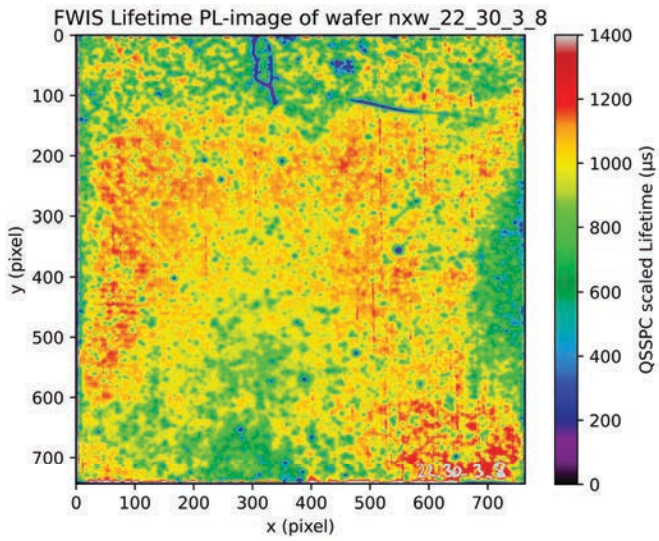

Figure 4: Photoluminescence measurement of an EpiWafer with 1 Ωcm resistivity

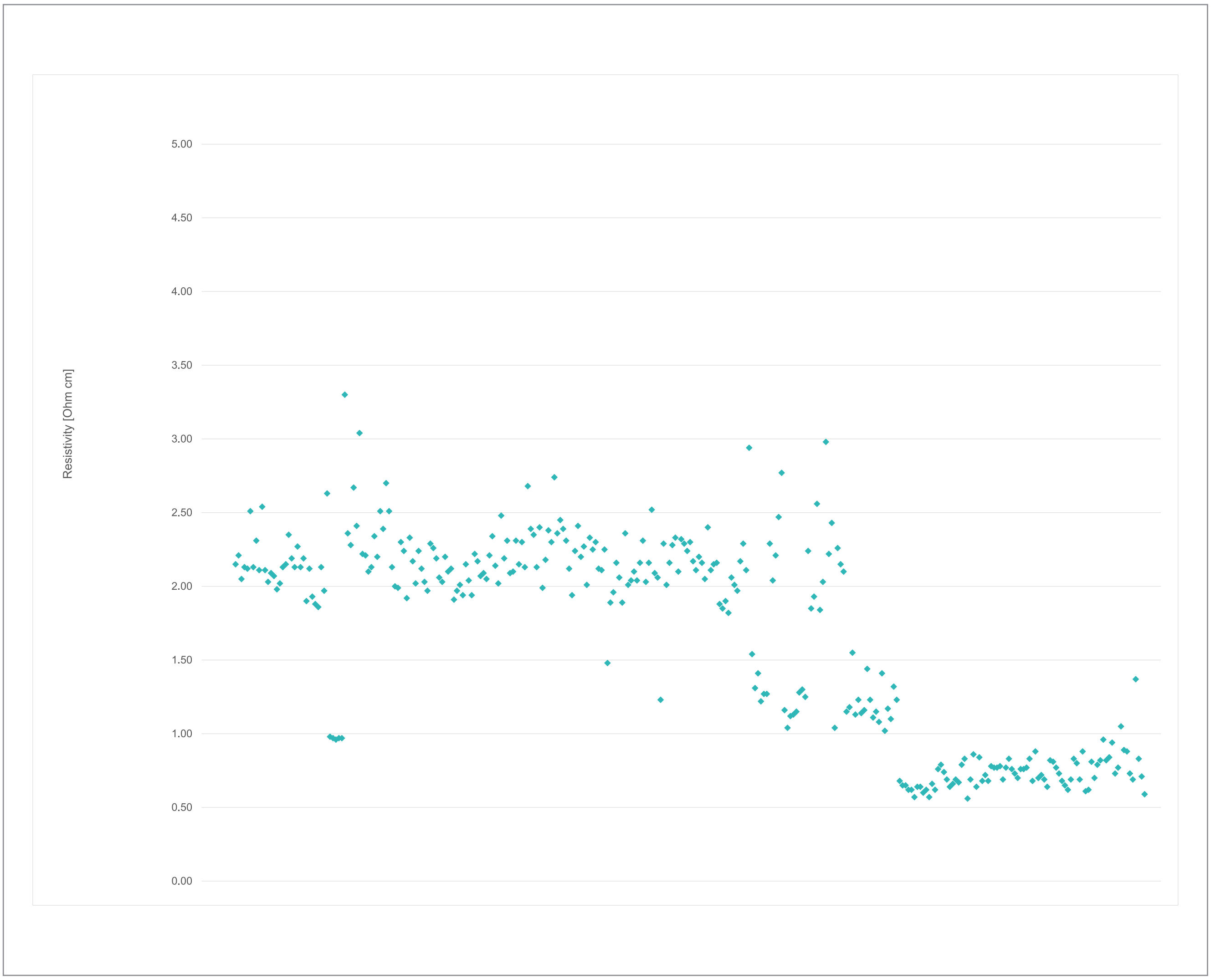

Figure 5: Resistivity of wafers grown by the EpiNex process

An advantage of the EpiNex process is its inherent flexibility regarding changes in wafer formats. It can cope with any wafer size as long as seed wafers of the same size are available and fit on the carrier system, which has an area of approximately 1 m2. The EpiNex process is fully compatible with all current wafer formats, but it is not exposed to the challenges of G12 manufacturing such as reduced ingot pull speed or lower energy efficiency.

Wafer thickness

NexWafe's EpiNex process offers an opportunity to produce the thin wafers that modern cell processes require, and the company has already demonstrated the production of wafers with a thickness of approximately 50 µm (see Figure 6).

The optimal wafer thickness depends on various factors, including the quality of the surface passivation and the quality of the wafer. For HJT cells, for example, the very good passivation at both the front and rear surfaces means that the optimum wafer thickness is below 100 µm. At PV CellTech 2022, Risen Energy calculated an efficiency gain of about 1% absolute for HJT cells by reducing the wafer thickness from 150 µm to 80 µm.

The ITRPV roadmap 2022 [15] predicts that the wafer thickness of conventionally produced wafers will drop to 125 µm but only over the course of 10 years, and further decreases are unlikely to be achievable for conventional wafer production at an acceptable throughput and yield.

While the use of thin wafers below 120 µm thickness requires advances in PV-cell manufacturing, in particular improvements in certain handling steps, 90–100 µm-thick wafers should be viable in cell and module manufacturing by 2026. The development will be driven by the need to unlock the true potential of high-efficiency cell architectures.

Carbon footprint

As discussed above, conventional wafer manufacturing has many inherently energy-intensive process steps and there is also high silicon waste due to kerf loss. The EpiNex process – a direct gas-to-wafer process – offers significant energy and carbon savings. In a comprehensive life-cycle assessment in 2020, Fraunhofer ISE compared the carbon footprint of EpiWafers with that of wafers manufactured using conventional manufacturing processes (polysilicon production by the Siemens process, Cz ingot pulling and diamond-wire wafer sawing). However, it must be noted that a like-for-like comparison should also take into account that EpiWafers have no saw damage. Thus, an EpiWafer with a 15–20 µm lower thickness than an as-cut Cz wafer gives the same solar cell thickness. Fraunhofer found that the EpiNex process offers significant potential for carbon footprint reductions (see Figure 7). The exact amount of the CO_2 footprint reduction is dependent on the site selected for manufacturing and the wafer thickness. Taking into account the compatibility of EpiWafers with very low wafer thicknesses, CO_2 footprint reductions of up to 70–75% were found to be possible. Even when comparing like-for-like in both manufacturing location and wafer thickness, the data from the study implies that CO_2 reductions of approximately 50% could be achieved.

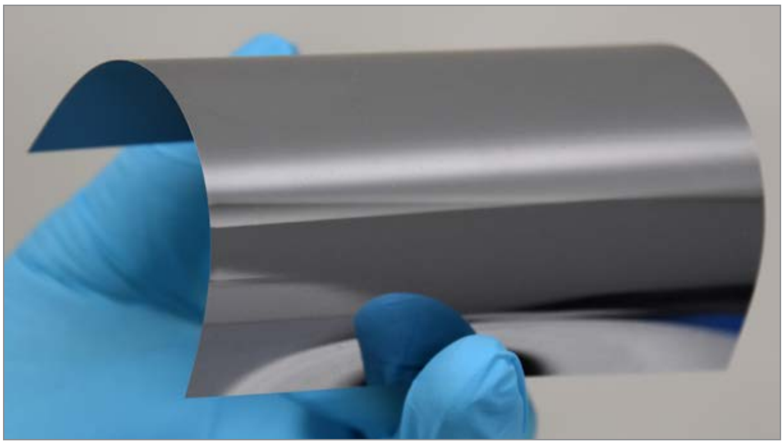

Figure 6: EpiWafer with 51 µm thickness

The increasing awareness of buyers and governments of the environmental impact and CO_2 payback time of PV modules will drive the industry to reduce its CO_2 footprint. Since almost 63% of the GHG emissions in module manufacturing stem from wafer production, the EpiNex process appears to be a clear opportunity

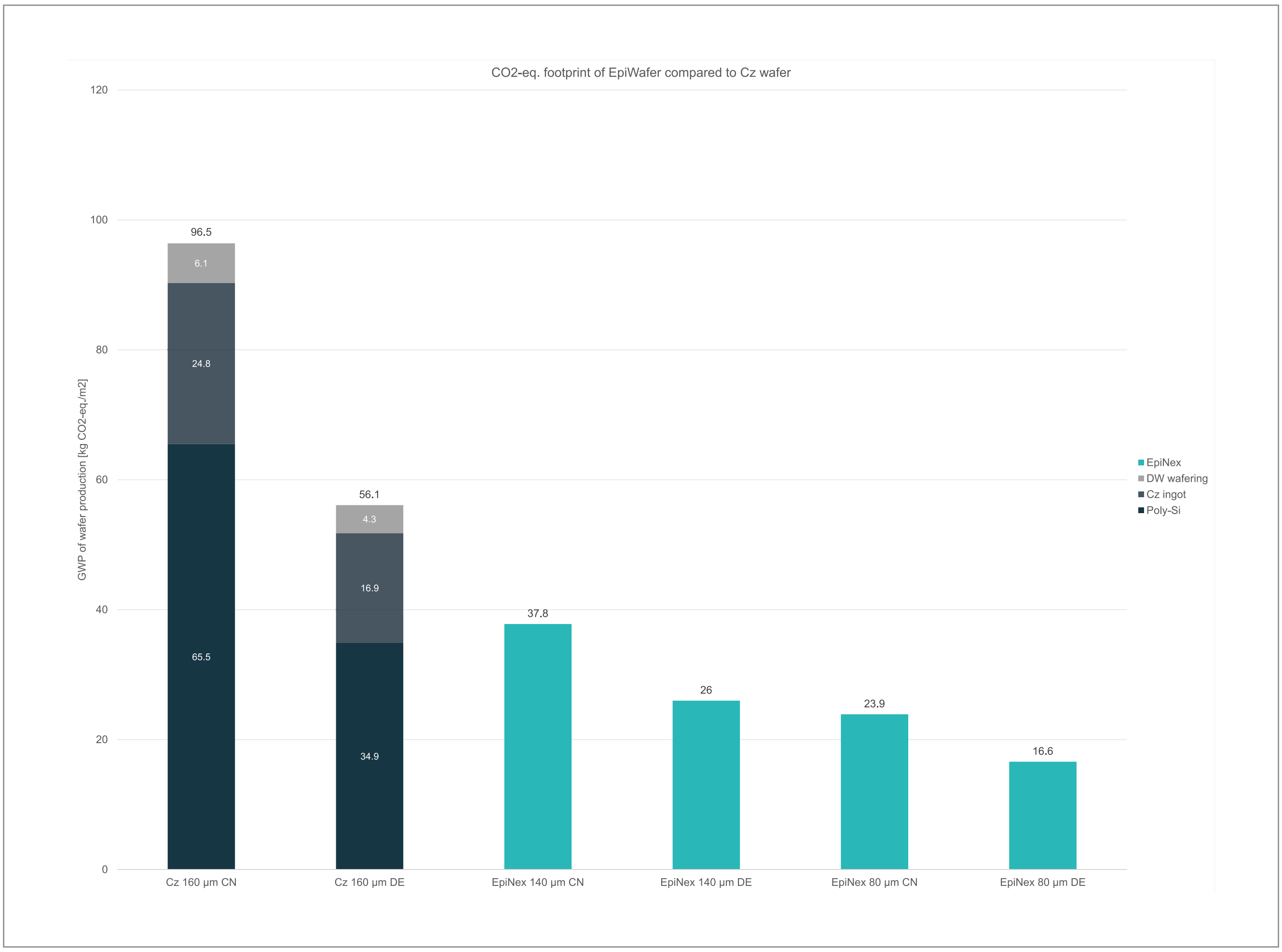

Figure 7: CO_2-equivalent footprints of the EpiWafer process versus conventional wafer manufacturing. CN refers to manufacturing in China; DE refers to manufacturing in Germany.

Source: Fraunhofer ISE

to reduce the GHG emissions of PV-module manufacturing by 30–50%. Using green solar EpiWafers would allow PV-module manufacturers to differentiate their offering from the competition and would help to accelerate the global reduction of GHG emissions.

Summary and outlook

Accounting for 60% of renewable capacity additions in 2021 [14], solar PV is moving fast towards becoming the single most important source of a sustainable global energy system. Nonetheless, expert projections are painfully clear in assessing that the current trajectory of the energy transition is nowhere near the Paris Accord's 1.5°C pathway. Reaching the required 5200 GW of installed solar PV capacity by 2030 – a seven-fold increase compared with 2020 levels – and over 14,000 GWp by 2050 for a net-zero scenario is a massive undertaking. But a mere focus on increasing installed capacity is not enough.

Current solar PV wafer-manufacturing techniques are costly and inefficient, with a significant carbon footprint. This is particularly true for the production of the most expensive and energy-intensive part of a module: the solar wafer.

Applying proven methods from electronics in its EpiNex process, NexWafe has set out to change that with a clear goal in mind: producing green solar wafers at scale for half of their current cost, with dramatically lower CO_2 emissions and superior quality.

The results derived from NexWafe's prototype production are very promising: oxygen impurity levels are an order of magnitude lower than those of Cz wafers, the EpiNex process has shown to be compatible with all current and upcoming wafer sizes – from M2 to G12 – and wafer thicknesses of down to approximately 50 μm have been reached. Also, the associated CO_2 emissions of EpiWafer production have been up to 70–75% lower than for Cz wafers, translating to a reduction in carbon emissions of 30–50% at a module level.

While it is clear that different manufacturing methods will coexist for the foreseeable future, NexWafe has many reasons to believe that its EpiWafers will be a highly competitive product that can help the PV industry to become greener and contribute to further reducing solar PV's levelised cost of electricity.

Backed by prominent industrial investors, NexWafe is planning to begin construction in 2023 on a 250 MW pilot production facility to demonstrate the commercial and technical specifications needed to meet customer requirements. With strategic partners, NexWafe will then be ready to move production towards the gigawatt scale.

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Pushing the limits of shingle heterojunction module performance, cost and sustainability

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Abstract

Recent developments have already proven the potential of shingle heterojunction modules, particularly adapted to new emerging PV markets where both high efficiencies and aesthetics are mandatory. Indeed, such an interconnection configuration can be easily applied on a large area and on high volumes with excellent overall module reliability [1,2,3]. But despite these very promising outcomes, silicon heterojunction (SHJ) shingle technology has not yet fully met expectations in terms of performance and cost competitiveness, mostly because of the SHJ intrinsic cell limitations. The efficiency losses linked to the cut-edge generated at cell level and the large amount of silver needed to compensate for the increased line resistance (deported busbar) are some of the remaining hurdles that need to be addressed to fully consider SHJ shingle for the next generation of PV products [4]. However, innovative and very promising solutions are proposed to tackle these limitations, and the main outcomes are detailed in this paper. Furthermore, the unique combination of SHJ and shingle allows a large window of optimisation at interconnection level, with the possibility to integrate thin and ultra-thin wafers, and also to drastically reduce the electrical conductive adhesive (ECA) consumption or cell-to-cell overlap, without impact on module performance. All these technological improvements contribute to enhancing the already high attractiveness of SHJ shingle technology, and to close the gap with industrial, economic and sustainability requirements usually considered for large-scale deployment of such panels.

Introduction

Shingle interconnection is gaining more and more interest as it combines high-efficiency potential and improved aesthetics due to the denser silicon integration within the final module panel [5,6,7,8]. Commercial products are already industrially available, mostly integrating PERC (Passivated Emitter and Rear Contact) cell technology (panels from Solaria or SunPower, for example). However, the latest high-efficiency PV cell architectures, mostly relying on a high level of passivation, are not an obvious match for such a module configuration. This is particularly the case for silicon heterojunction (SHJ) devices, for which optimised integration needs to overcome two major intrinsic limitations:

1. High efficiency losses after cell cut in shingle stripes (up to 1% Abs losses can be observed on final cut-cells).
2. High metal resistance linked to the deported busbar metal pattern, and the high resistivity of low-temperature silver metal paste.

While it has already been demonstrated that high-performance shingle modules with excellent reliability can be manufactured with SHJ-based cells [9], it is clear that innovative solutions are needed to further enhance the attractiveness of such SHJ shingle modules. This is true not only for costs, but also for overall long-term sustainability of the technology, which cannot be neglected if very large volumes of such modules are expected in the coming years [10]. So, how can the current limitations highlighted for our SHJ shingle modules be further addressed?

Firstly, at cell level, we will show that significantly higher efficiencies can be achieved with the application of highly promising post-cut-edge repassivation solutions. Indeed, we demonstrate that a low-temperature AlOx layer with a proper activation process could lead to more than 90% performance recovery. SHJ shingle cut-cells fabricated with such an edge-passivation process reached efficiencies very close to the mother cell before cut. To address the metal resistivity issues, an increased amount of silver paste is generally deposited to reach a sufficiently high final line aspect ratio. This is obviously not acceptable and we will show that a switch towards copper metallization solutions seems unavoidable in the near future.

Secondly, we will also show that due to the unique properties of the SHJ architecture, there is still room for optimisation at both interconnection and module levels. The excellent adhesion of ECA (Electrical Conductive Adhesive) on the cell TCO (Transparent Conductive Oxide) allows, for example, a drastic reduction of ECA consumption and/or the move towards very aggressive cell-

"...significantly higher efficiencies can be achieved with the application of highly promising post-cut-edge repassivation solutions."

to-cell overlap (down to 0.5mm, as shown in this paper). Furthermore, the symmetric and low-temperature configuration of the SHJ makes it particularly compatible with the use of thin and ultra-thin wafers, and very promising modules integrating 120μm- and 90μm-thick wafers have been generated, all showing even better reliability outputs than the reference modules built with standard 160μm-thick cells!

High efficiency, aesthetics, low cost and sustainability…can we really have it all? Compromises will probably be needed, but as we will show in this paper, with such progress margins left at both cell and module levels, we confirm that the already huge potential of the SHJ shingle technology can be even further optimised to propose high-quality products complying with industrial, commercial and environmental requirements in the near future.

An already mature technology

As shown in a previous PVI-dedicated study [3], large-area modules integrating shingle heterojunction cells have been successfully manufactured in collaboration with Applied Materials–Baccini for the stringing part. Electrical output powers of up to 400W were measured on the best modules [11], but it was also recently shown that extremely good technology repeatability could be achieved with production of higher volumes of panels, all showing very similar power outputs. This is the case, for example, for the modules presented in figure 1, where smaller module sizes were targeted (60 M2 equivalent final dimension) in a glass–glass configuration. As shown with the final power measurements, all modules built are functional, but the most impressive aspect is the high uniformity of the performance achieved, proving the very good repeatability of the whole fabrication process (from initial cell to final module). The slightly better output powers observed for the first two modules are only linked to the lower optical wavelength cut-off encapsulant used for these modules, allowing in particular an increase of the UV (Ultra Violet) light harvesting within the panel.

Such outcomes are still obtained while maintaining very high reliability, with limited power losses for up to 800 TC (Thermal Cycling aging tests conducted between -40°C and +85°C), which is impressive and even better than what is generally observed for standard ribbon interconnection SHJ panels. It can be seen that such good reliability results are maintained even when using significantly thinner wafers within the module. The specific case of thin-wafer integration will be detailed in the next section. It is also important to observe that high bifaciality has been maintained on the fabricated shingle modules (typically ~85% bifaciality) and this can be key if the final applications will benefit from a high level of albedo once installed. Indeed, the first monitoring data extracted from such bifacial modules clearly show the benefit of the high-performance SHJ shingle modules when compared with other technologies such as PERC, for example. The higher performance ratio (PR) demonstrated is also linked to the better module bifaciality coefficient, demonstrating that even for shingle configuration, increased performance can be observed with proper management of the back of the module.

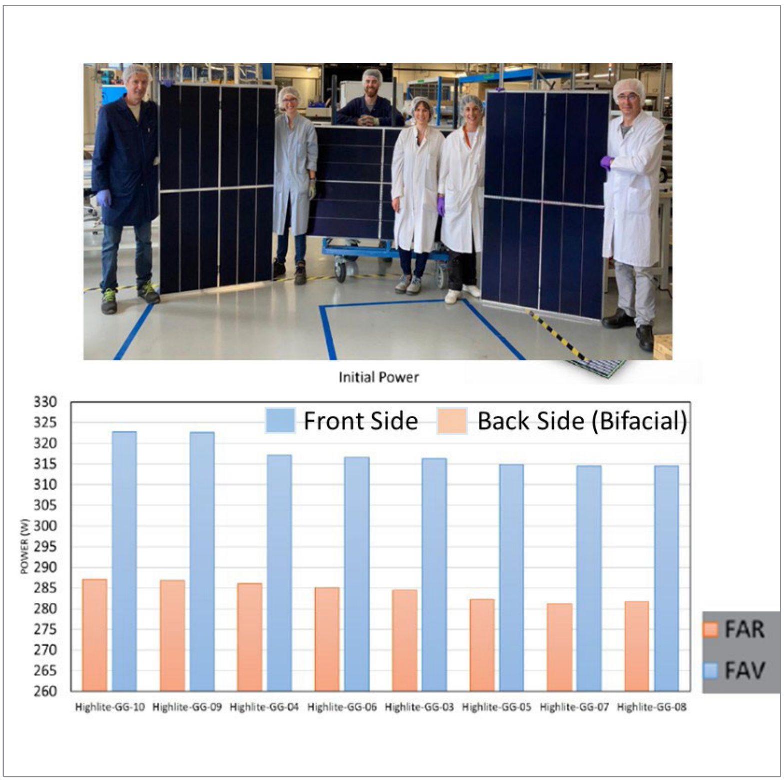

Figure 1: SHJ shingle module typical mini-production batch outputs. Top: Picture of the CEA-INES module research team with large area shingle modules as manufactured on the pilot-line. Bottom: Ouput power (in W, front and back-side illumination values provided) measured for the latest SHJ shingle panels produced, showing extremely high repeatability and uniformity of performance.

Possible improvement remains at the interconnection level

Even though very promising outputs have already been demonstrated for an SHJ shingle configuration, the latest developments conducted at CEA-INES showed that there is probably still room for further improvement, especially at the interconnection level.

Firstly, due to the very good adhesion of ECA observed on the upper TCO layer, we tried to reduce the total amount of ECA deposited on each individual shingle tile. Indeed, even if low quantities of ECA are considered, the current price of such products remains high. Consequently, if even lower amounts of ECA could be achieved

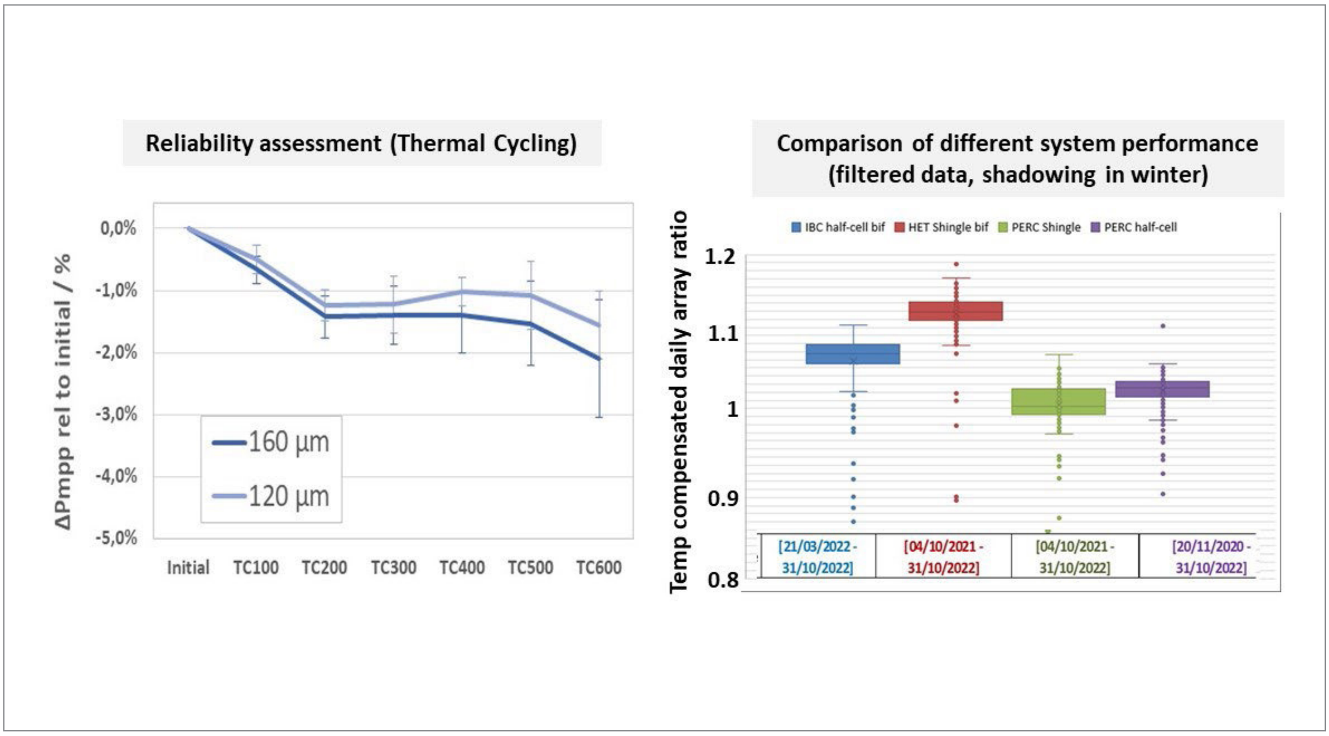

Figure 2: (Left) Outstanding reliability demonstrated for SHJ shingle modules, even for thinner wafers. (Right) Temperature corrected performance ratio (PR') for several module strings monitored at CEA Cadarache, showing improved performance for the SHJ shingle modules, due to both high initial performance and the high bifaciality coefficient of the module installed.

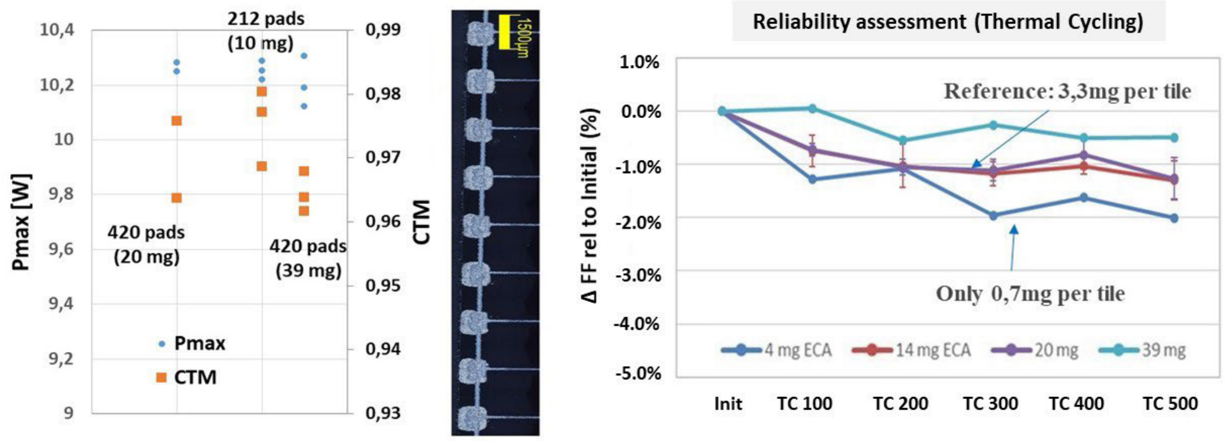

Figure 3: Impact of the deposited ECA mass for shingling. (Left) Negligible impact on mini-module performance (Pmax) of ECA reduction. (Right) Very high reliability maintained even for the very low deposit conditions.

without any impact on either module performance or overall reliability, this would help to further reduce the cost of the final product. Experiments were conducted on mini-module configuration, varying the ECA weight between high-deposit conditions (39mg per full cell, so ~6.5mg for a single tile) to very low deposits (only 4mg per full cell, so only ~0.7mg for a single tile). The typical ECA deposit for a standard module is 20mg for each full cell, so approximately 3.3mg for each individual tile. As shown in figure 3, negligible impact on module performance is observed when lowering the ECA amount deposit, which is a promising outcome, meaning that the series resistance is not increased with the reduced quantity of paste used. Besides, the most outstanding results come from the monitored reliability, as extremely good module performance is maintained for all ECA deposit conditions. Even if the highest ECA deposits feature slightly improved reliability after TC (Thermal Cycling) aging tests, less than 2% relative fill factor (FF) losses can still be achieved after up to 500 cycles even for the lowest ECA deposit. Power losses (not shown in figure 3) follow the same trend, with again less than 2% relative losses for up to 500 cycles, which remains well below the usual normative threshold of 5% power loss tolerated.

Secondly, in addition to ECA optimisations, another way to address cost issues is to evaluate whether more aggressive cell-to-cell overlap could easily be achievable for the interconnection scheme. Indeed, with reduced overlap, higher module power could be achieved due to the increased PV conversion surface, which will ultimately lead to lower costs (more W for a similar cell and module material cost…). Again, several mini-modules were processed, varying the cell-to-cell overlap from 1mm (the standard value for our developments) to a very aggressive value of only 0.5mm. This reduction was very challenging, as for such a small overlap, very accurate alignment must be ensured for many successive processes: cell metal print, cell cut, ECA deposition and cell positioning on final strings. Initial experiments showed an increased number of failures during module fabrication. SEM analysis of the interconnections (figure 4) showed that while reducing the overlap, the ECA was spreading over the edge of the cell, leading to electrical shunts. However, on the working modules, there was clear evidence of a power improvement due to the reduced overlap, mainly linked to the increase of the current\ to the increased PV surface, as expected. However, even if reliability remains within the usual normative requirements for such modules, a clear degradation is measured in thermal cycling tests when shifting from 1mm to 0.5mm. To overcome these issues, it was decided to modify the metal busbar pattern design, allowing extra open space between two successive tiles and relieving the alignment constraints for ECA printing. If aggressive alignment constraints still occur on the stringer cell placement, this simple optimisation significantly improves both manufacturing outcomes (higher numbers of fully functional modules generated) and reliability. As shown in figure 4, the reliability gap between reference modules and 0.5mm overlap modules

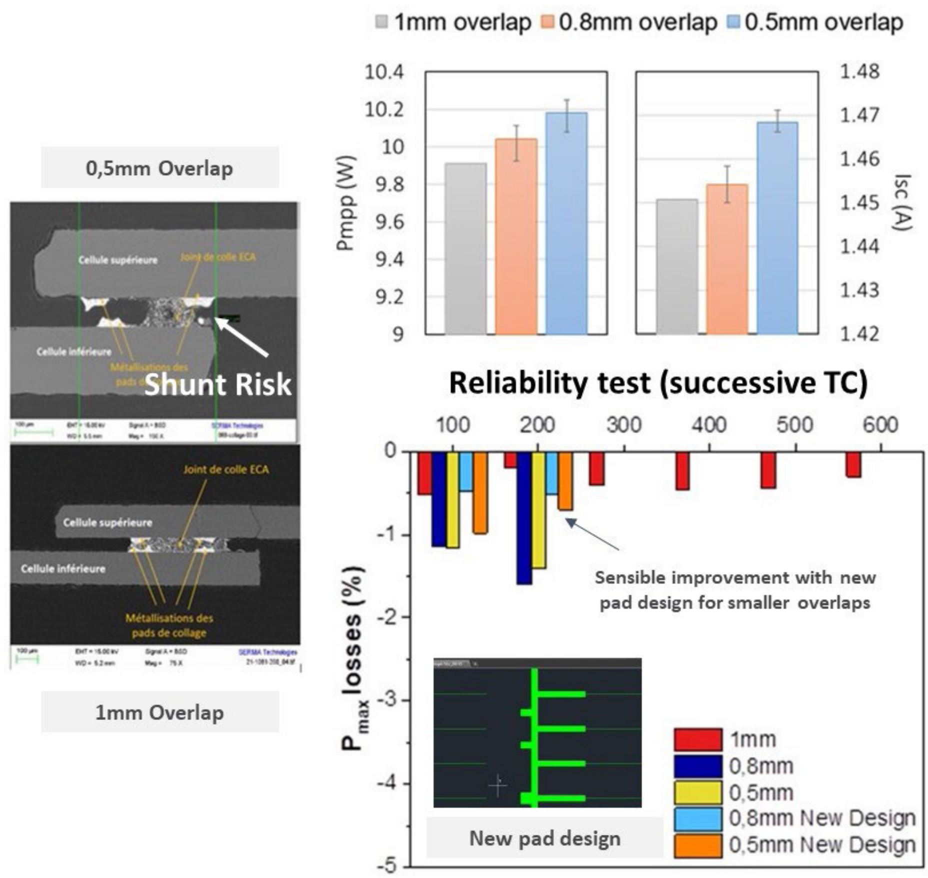

Figure 4: Impact of cell-to-cell overlap reduction. (Right) SEM pictures highlighting the increased shunting risk with reduced overlap – (top) Pmpp improvement shown at module level for reduced overlaps; (bottom) reliability assessment of different overlap configurations. Good reliability maintained for the 0.5mm overlap with newly adapted metal design.

has been significantly reduced, and promising preliminary results are demonstrated up to 200 cycles (less than 1% power degradation for the 0.5mm overlap case). Nevertheless, there is still optimisation work to be done to fully consider the 0.5mm overlap for production. In the meantime, a 0.8mm overlap seems fully compatible with all integration constraints and could already be a significant lever for improvement of the technology.

Sub-120μm wafer integration in shingles

Thin-wafer integration has been a major achievement for SHJ shingling technology. The symmetrical architecture of SHJ makes it possible to achieve high performance even on very thin wafer substrates, as demonstrated by several studies conducted at CEA-INES and very recently by LONGi, with an impressive efficiency of 25.68% obtained on 56μm-thin wafers presented during WCPEC-8 [12]. For shingle evaluation, we screened three different wafer thicknesses: standard 150/160μm wafers, thinner 120μm wafers and very thin 90μm wafers. The objectives with such thin wafers were to assess the feasibility of shingle integration and to open up a new field of applications due to the extra flexibility of the wafers. Furthermore, the use of thin or ultra-thin wafers is consistent with cost reduction and increased global sustainability goals, where wafers are a major contributor in both cases.

Work has been conducted, first, on 120μm-thick wafers, with very promising outcomes, as already shown in figure 2. Fully operational large-area modules have been manufactured, with the thermal cycling qualification passing 3xIEC standard requirements. Then, a set of mini-modules was produced, integrating all three main wafer thicknesses mentioned, with the main objective this time to assess the impact of even thinner wafers, down to 90μm. These ultra-thin shingle cells were all processed on the CEA-INES production pilot-line, with a promising 22.2–22.3% average range efficiency achieved. Even though the volume produced remains small, with such medium-scale processing conditions no increase in breakage rate was observed during either stringing or lamination. However, the laser-

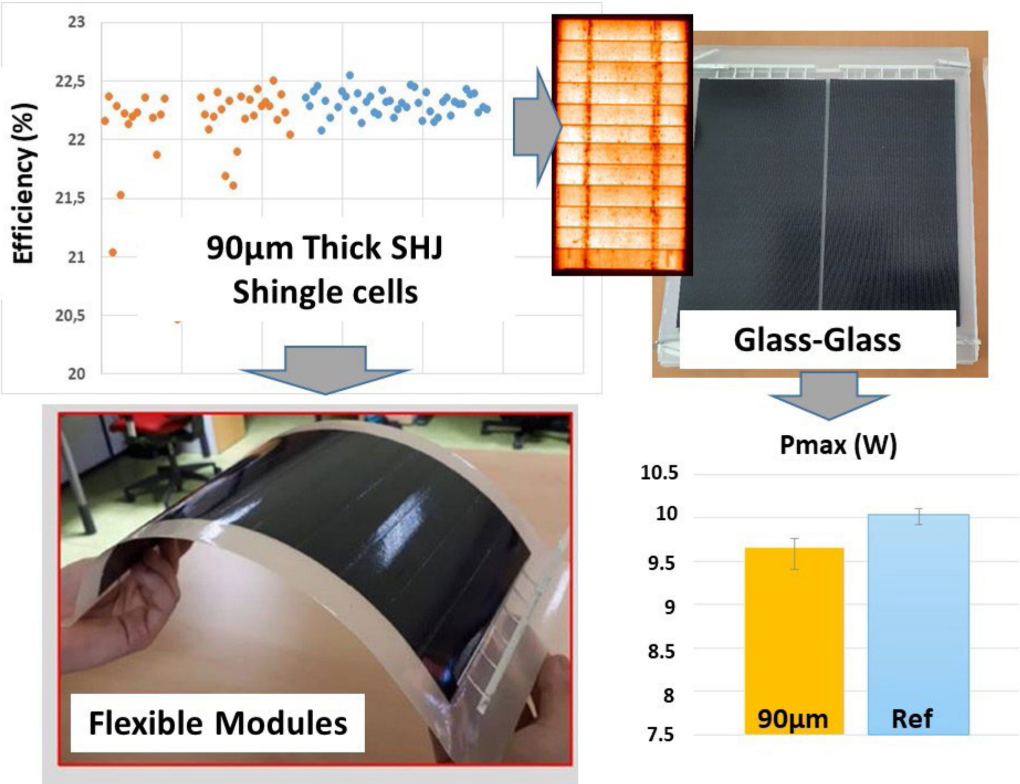

Figure 5: Illustration of different cell and module outcomes integrating 90µm-thick SHJ shingle cells. (Top left) Typical efficiencies achieved on the production line with 90µm wafers. (Bottom right) Typical mini-module output powers achieved for 90µm wafers and compared with the usual 150µm reference.

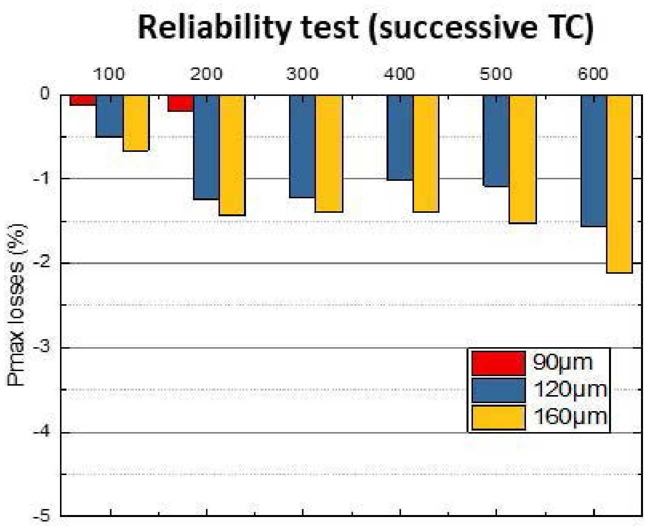

Figure 6: Thermal cycling reliability assessment for modules integrating different wafer thicknesses (glass–glass configuration). Improved reliability was demonstrated with a reduction of the wafer thickness integration for the SHJ shingle module configuration.

cutting process had to be slightly adjusted to ensure a low breakage rate during the cut of the initial full cell into six shingle tiles.

Module results achieved were in line with expectations, with final output powers slightly below the 160µm reference for the modules integrating the 90µm wafers, mostly due to lower initial full cell efficiencies. But similar Cell to Module (CTM) values have been calculated, showing that no degradation of the interconnection quality in particular was observed after integration. Furthermore, electroluminescence (EL) observations did not reveal any cracks or degradation within the module upon processing. In parallel, low-weight and flexible modules were specifically designed using an adapted bill of materials for module assembly. Several modules were produced again in these conditions, combining a high degree of flexibility and very pleasing aesthetics, as shown in figure 5. These modules benefit from the intrinsic strength of the shingle interconnection due to the superior mechanical properties of ECAs and their strong adhesion on the TCO layer. So, SHJ shingle technology, coupled with the increased flexibility of thin wafers and a carefully selected bill of materials, could clearly pave the way towards many novel PV module applications.

Finally, reliability tests were conducted on the mini-modules in a glass–glass configuration with different wafer thicknesses, as presented in figure 6. A power loss well below 5% was observed for up to 200 cycles, which was maintained up to 600 cycles on 120μm and 160μm wafers. Moreover, the most impressive result is the fact that the power loss was reduced even when reducing the wafer thickness. This very impressive result was probably achieved due to the higher degree of flexibility of the thin wafers, which can better absorb the mechanical mismatch induced by the successive thermal cycles conducted during TC (further measurements are in progress). According to these preliminary results on thin wafers, a completely new progress path for shingle SHJ technology was evidenced, in terms of potential for cost reduction, improved reliability and alternative applications.

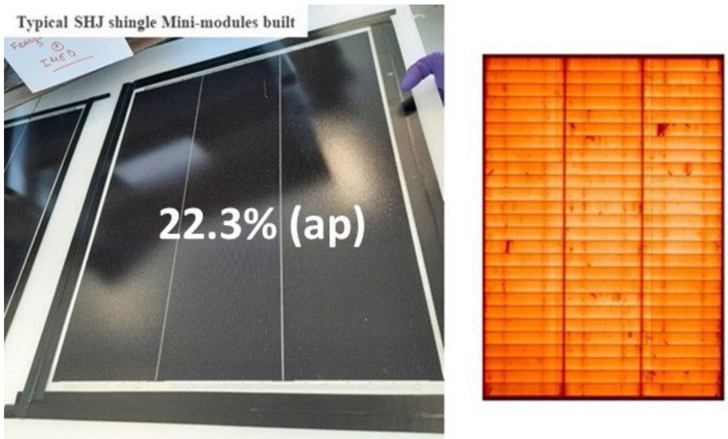

Figure 7: Photo (left) and EL (right) of a module prototype (three strings of 26 tiles) demonstrating the capability of reaching a high efficiency of 22.3% (aperture measurement) for the SHJ shingle configuration. Performances are still mostly limited by cut-edge parasitic recombination (no edge passivation on the integrated tile for this module).

Efficiency boost with a cell edge-passivation process

As shown in the previous sections, promising module powers and efficiencies are already achievable with current cell and interconnection processes. Also, a very promising 22.3% module efficiency was obtained recently on medium-size modules (figure 7). However, as mentioned previously, a significant performance loss is still observed because of the edge defectivity generated during the full cell cut in smaller shingle dimensions [13]. This is particularly a problem for the SHJ architecture, which generally presents a very high Voc on full cells, due to the high quality of passivation of the amorphous layers used.

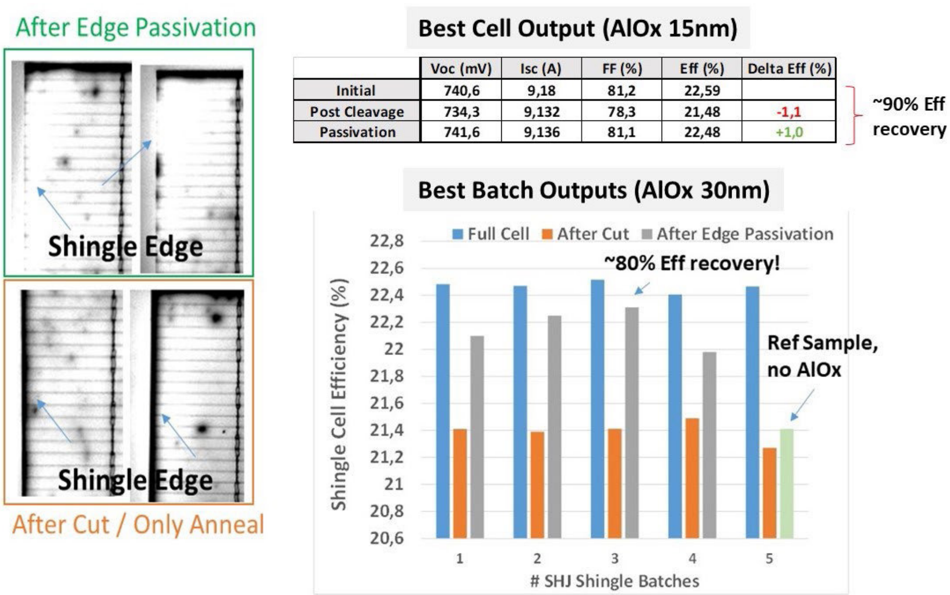

Figure 8: The low-temperature AlOx-based edge-passivation process developed. Significant improvement of the edge PL signal is observed, which translates to high recovery of performance as measured on the cut-shingle cells after deposition of the passivation layer. Up to 90% performance recovery was demonstrated on the best cells.

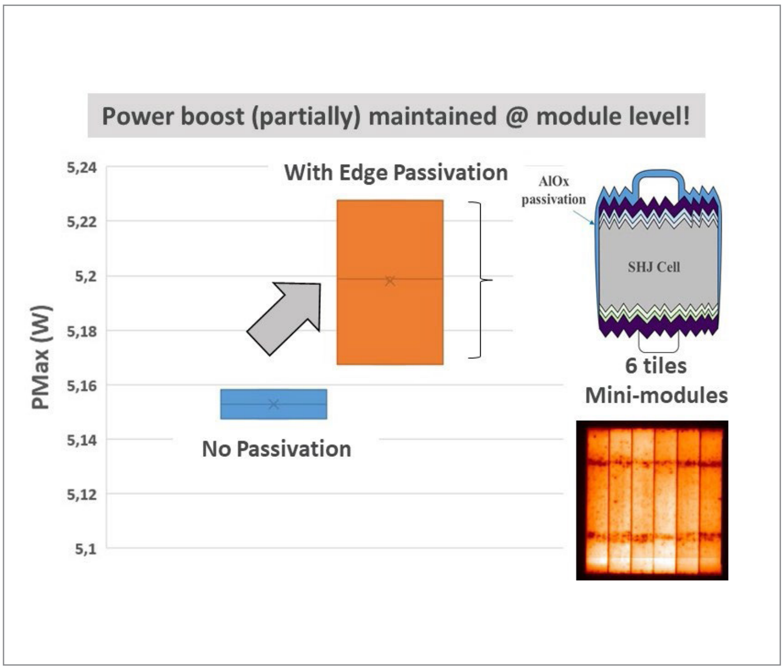

Figure 9: Average performance measured for glass–glass SHJ shingle mini-modules (three modules for each configuration), highlighting the performance improvement achieved with the integration of the passivated shingle tiles (as illustrated in the schematic on the right). No apparent degradation of interconnection quality was observed, as shown, for example, on the PL image provided.

To improve cut-cell performance, an additional edge-passivation process is required [14,15]. At CEA-INES, we have developed low-temperature (~100–130°C) aluminium oxide (AlOx) layers, deposited by Atomic Layer Deposition (ALD) and compatible with the SHJ architecture constraints. The annealing and activation of the deposited layers is ensured by optimised light-soaking treatment, which is a process already widely implemented in most SHJ production lines. Details can be found in [16] and only the most representative results will be reported in this paper. With a fully optimised process, we demonstrated that highly significant efficiency recovery is obtained on the shingle cells undergoing such an edge-passivation process. This is clearly shown on photoluminescence (PL) observations and also on cell electrical outputs, with up to 90% performance recovery demonstrated for the best devices. The repeatability of the process described in this paper has also been proven on repeated batches, with higher volume of cells processed (more than 100 cells processed in total), proving the robustness of this passivation process. Further developments are ongoing to improve the AlOx layer quality and its industrial compatibility, by reducing the layer thickness and increase even further the passivation potential. Transferring the layer deposition from ALD to Plasma Enhanced Chemical Vapor Deposition (PECVD) tools is also an objective to reach high-volume wafer treatment, as required for the PV industry.

The passivation quality of this process was demonstrated with AlOx layers down to 15nm and, as mentioned previously, work is ongoing to further reduce this thickness. This is important, as, for now, the process consists of full-wafer deposition of the layer, meaning that this insulating AlOx covers both TCO and metal, and could potentially degrade ECA adhesion or overall interconnection conductivity. This must be properly assessed, and to that purpose, a set of dedicated mini-modules has been built, integrating shingle SHJ cells with the AlOx passivating layer. EL characterisation conducted on finalized modules do not show any apparent degradation of the quality of the interconnection with these devices (figure 9). This was only partially confirmed by IV electrical measurements. Indeed, an improved output power was shown for all the modules with cell edge passivation, which is the first confirmation that performance improvement achieved at cell level can be maintained at module level. Power gain is linked to both improved FF and Voc on the passivated modules, as expected. However, modules with a passivated edge also showed a greater performance dispersion than the reference modules, indicating that further integration optimisation is still probably needed to tackle the additional challenge brought by the presence of the AlOx layer and then to fully profit from the higher initial cell efficiency potential. Results presented are nevertheless very promising, as this is the first experimental validation that the passivation process proposed in this paper should be suitable with all cell and module production constraints. New experiments are planned and an overall reliability assessment of the module produced will be performed during the next few months.

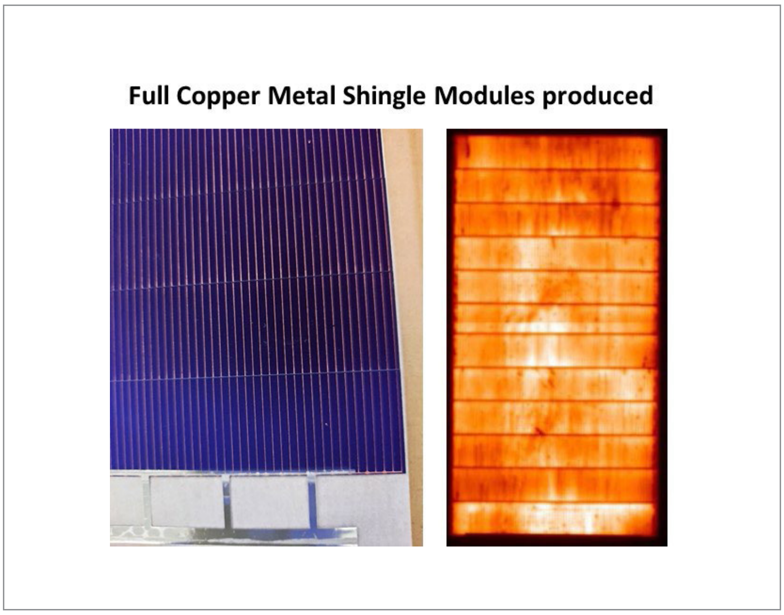

Figure 11: The first SHJ shingle modules successfully assembled with full copper-paste metallization

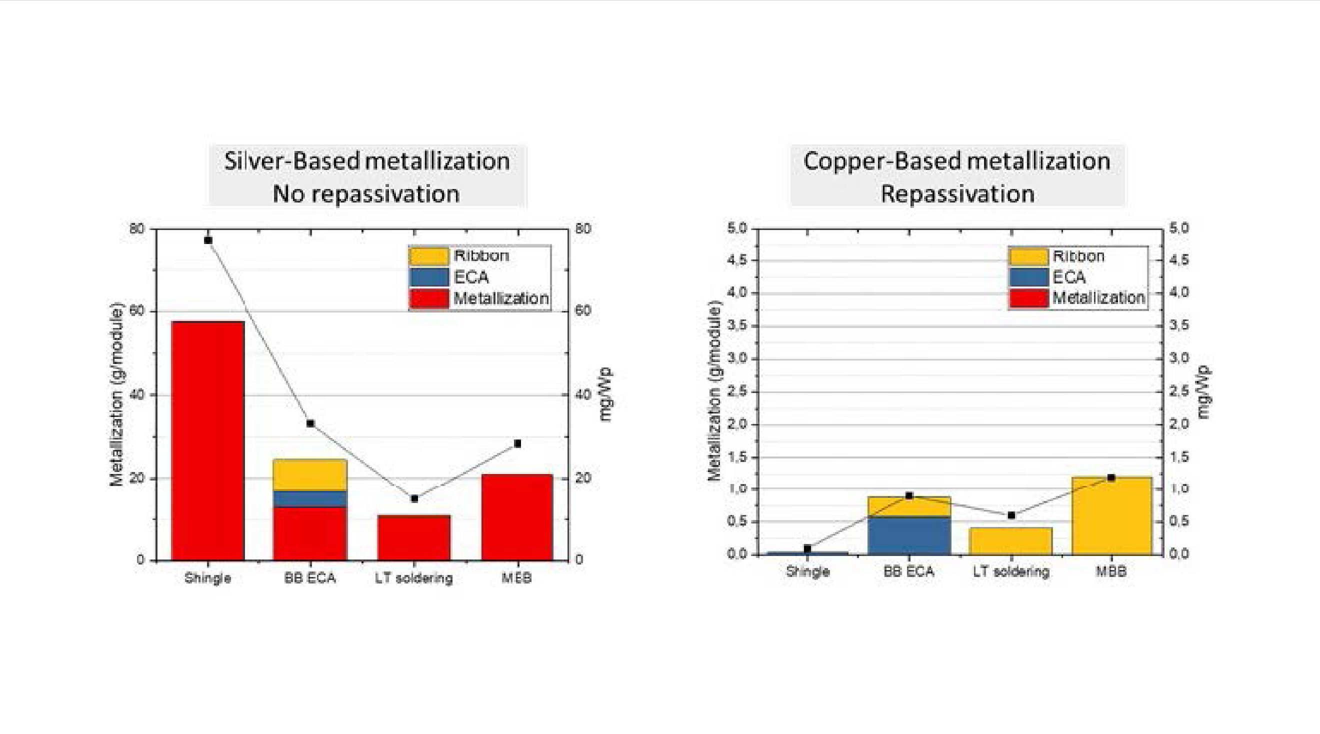

Figure 10: Projected silver consumption for different module cell and interconnection configurations. A switch to copper metal solutions is clearly beneficial, especially for an SHJ shingle configuration, which becomes highly competitive compared with other technologies.

Towards copper-based shingle metallization?

It has already been shown in previous sections that silver usage at interconnection level can be reduced to very low deposits without impacting the quality of the interconnection. However, the main silver consumption will remain in the cell, as a larger amount of silver is needed to compensate for the shingle-specific metal grid design. Indeed, with the deported busbar, the length of the metal lines is approximately twice the length of conventional cells and the impact on performance is tremendous if no specific optimisation is applied. The current SHJ shingle technology is thus significantly impacted in terms of cost competitiveness with regard to the usual alternative module solutions (Figure 10). Even though progress has been made recently in the reduction of silver-paste deposits, the amount of silver needed to maximise cell performance will always remain greater than that needed for more usual cell architectures (busbar SHJ, TOPCon, PERC, etc). Consequently, a switch to an alternative metallization scheme seems unavoidable and the most promising candidate for now is the switch to copper, either using copper paste or introducing copper plating [17].

But, is this really an issue for the future of shingle? Probably not. Indeed, for any solar cell technology, as made clear by several recent publications, the use of silver for metallization will not be possible for the Terawatt-scale production projected over the coming years [18] and a shift of the whole solar industry towards a silver-free metal solution will happen over the next few years. As shown in figure 10, this will benefit even more the SHJ shingle configuration. With proper management of the edge-related performance losses (see previous section), projected simulations/calculations suggest that the shingle module configuration can actually become the most attractive in terms of overall sustainability and once again become very attractive cost-wise.

Still, is a shingle interconnection compatible with copper? We successfully achieved the first functional modules integrating SHJ cells produced with copper-paste metallization (as shown in Figure 11). If this preliminary result shows the compatibility of full copper metallization with a shingle configuration, dedicated reliability tests conducted (not shown here) indicate a significant degradation of performance after only a few thermal cycles, probably linked to uncontrolled oxidation of the copper. Further optimisation is thus needed, and new tests are required with alternative copper pastes (or copper plating) and adapted ECA. The most promising combination(s) should be identified soon, and shingle modules will also benefit from general progress in copper integration in a standard module interconnection configuration.

Conclusions

In this paper, we provide an overview of the current status of SHJ shingle developments conducted at CEA-INES, in collaboration with Applied Materials–Baccini for the stringing part. Although the technology developed already shows a high degree of maturity and industrial readiness, which is also confirmed by the improved first outdoor monitoring outputs generated, there are still challenges to overcome to realise the full potential of the technology and to propose a cost-effective final product adapted to market constraints. Among the remaining challenges to address, there is the proper optimisation of the cut-edge performance losses and work on global silver-consumption reduction. For edge passivation, a very promising process path is already under development. In terms of the metal concerns, the SHJ shingle configuration will probably need to switch to copper solutions, but this would probably be the case for most of the alternative PV architectures as well. We also showed that the current interconnection scheme could still easily be further optimised to enhance its performance and address cost of fabrication issues. Very impressive results were obtained at module level with extremely low ECA deposits, down to only 0.7mg per tile as demonstrated in this paper. Another major achievement confirmed in the global work presented is the extremely high reliability of the SHJ shingle interconnection developed. Finally, we also highlighted the high (and unique?) compatibility of this SHJ shingle technology with the integration of thin and ultra-thin wafers (down to 90µm). Excellent output powers and impressive reliability were obtained on the different modules produced, opening up a whole new field of potential applications for the technology in the future.

Acknowledgements

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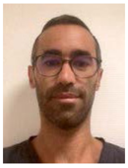

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Options for Upscaling of Perovskite-Silicon Tandem Solar Cells

Oliver Schultz-Wittmann, Martin Hermle, Baljeet Goraya, Sebastian Nold, Patricia Schulze and Juliane Borchert, Fraunhofer ISE

Abstract

The efficiency of crystalline silicon solar cells is reaching its practical limit in R&D as well as in high-volume manufacturing. To further drive down the cost of electricity produced by photovoltaics, increasing the efficiency beyond the limit for single-junction crystalline silicon is strongly desirable. 2-terminal perovskite-silicon tandem solar cells represent an appealing option: they benefit from the installed manufacturing capacity and process maturity of the silicon bottom cell, and achieve the high efficiency potential by adding a thin-film top cell. The first lab results with efficiencies of more than 30% have recently been announced [1]. Naturally, such champion devices are initially produced on small areas of the order of 1 cm2 and to date not all of the fabrication methods used in the laboratory meet the challenge of scaling up to industrial production. In this paper we discuss recent advances in the field, with a focus on potential device designs and manufacturing processes.

Introduction

The PV industry is expanding to ever-larger manufacturing capacities and crystalline silicon has taken the largest market share, marginalising competing thin-film technologies during this expansion. The ability to deliver a high power conversion efficiency has been a crucial factor leading to this success story. A high power conversion efficiency reduces the overall levelised cost of electricity, which – together with the low degradation rates – are the central metrics with respect to investment decisions. With the achievable efficiency of crystalline silicon solar cells approaching the practical limit, further improvements can be achieved by increasing the number of light-harvesting absorbers. In this way, different sub cells, whose band gaps are tailored to the incident solar spectrum, can selectively harvest the photons and more efficiently transform the photon energy into electricity. Such multijunction cells have successfully been developed in R&D and are in commercial production for space applications and concentrator technology. While crystalline silicon has a fixed optical band gap, thin-film technology offers the ability to tune the band gap for the desired application. Therefore, the combination of crystalline silicon and thin-film technology could be the technology of the future.

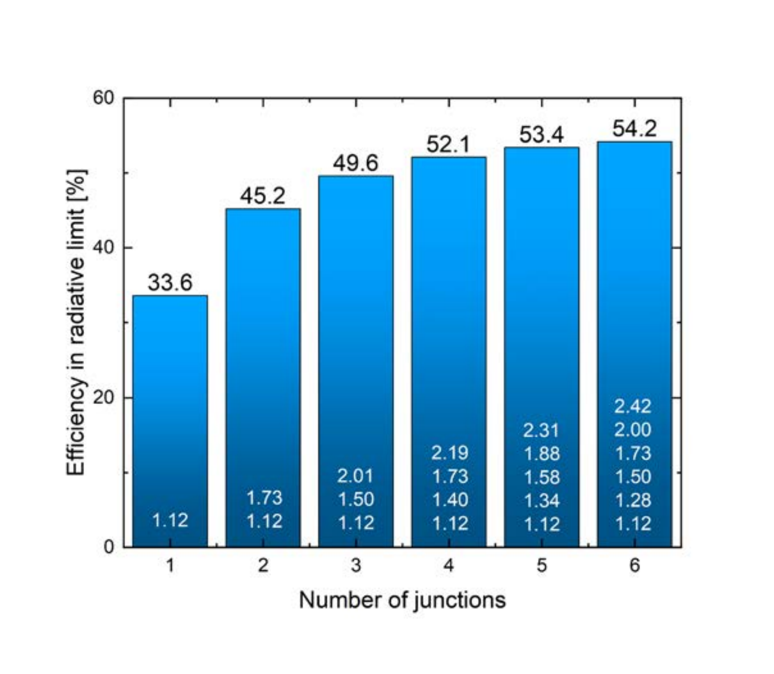
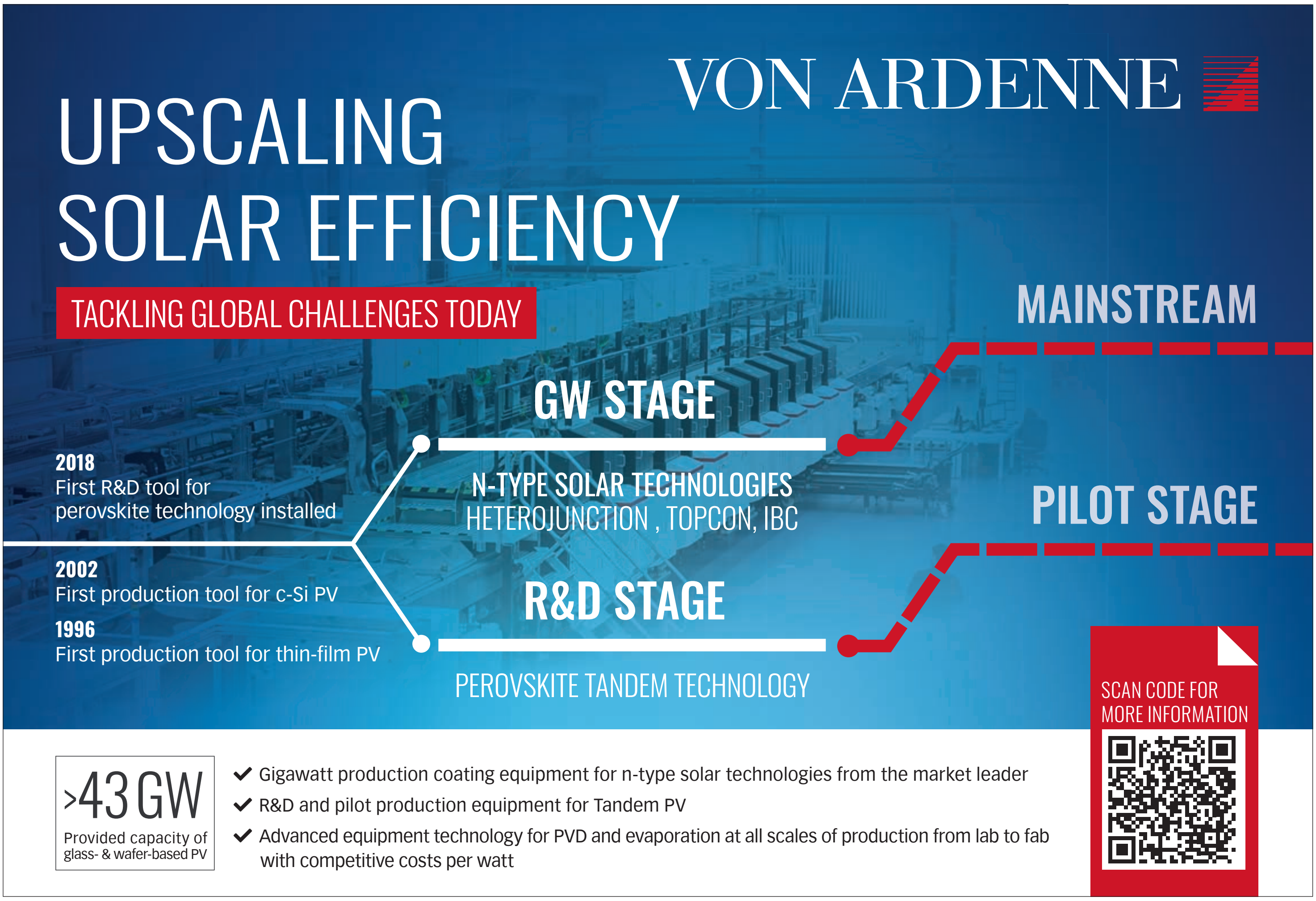


Figure 1: Obtainable efficiency in the radiative limit for crystalline silicon solar cells and multijunction cells with a crystalline silicon bottom cell. The white numbers inside the columns provide the optimum band gaps for the sub cells. Graph: provided by Patrick Schygulla; see also [2].

One of the upcoming tasks is to select the best thin-film technology for combination with crystalline silicon. In recent years, the perovskite material class has attracted significant attention due to, first, the ease with which the band gap can be tuned by adjusting the composition and, second, a rather high defect tolerance. Also, it is potentially a low-cost technology because metal halide perovskites can be deposited from abundant materials using low-temperature processes and therefore it is at the centre of development efforts in academia and industry. In its simplest implementation, the multijunction concept uses two junctions and the result is a so-called tandem cell. This already offers a major increase in the theoretically achievable efficiency considering the radiative limit, which is boosted from 33.6% for a single-junction crystalline silicon solar cell to 45.2% for a tandem cell based on a crystalline silicon bottom cell (see Figure 1). By adding further junctions, the increase in efficiency becomes less pronounced. The practical efficiency limit of such multijunction concepts will also be governed by the losses arising from the need for optical and electrical coupling between the sub cells and the increasing process complexity and costs.

Also, a choice needs to be made for the electrical contacting scheme. In principle, every sub cell can have its own electrical contacts (one per polarity)



for connection in a PV module. For a tandem cell, this would be a 4-terminal device in which the sub cells are only optically coupled to each other. There is also a configuration where the two cells share a common contact, hence resulting in a 3-terminal device. Alternatively, a 2-terminal tandem is an option, where, similar to a silicon solar cell, the electrical energy is only extracted at two external contacts and where the current generated in the sub cells should be identical for optimum performance (see Figure 2).

While the latter condition – matching of the current in both sub cells – imposes some technological constraints, it is the least complex configuration when connecting several cells in a PV module. Hence, 2-terminal tandem cells with a crystalline silicon solar cell on the bottom are a natural starting point and are the focus of this article.

Device architecture of 2-terminal tandem solar cells

When integrating two sub cells with different band gaps into a single device, the cells need to be adjusted to each other because in a 2-terminal device the cells are not only optically but also electrically coupled. In the following, we address the choice of the bottom cell and the individual layers of the top cell. For example, Figure 3 shows a schematic sketch of a perovskite-silicon tandem cell with an HJT bottom cell.

Bottom cell

There are several choices for the bottom cells, even when constraining ourselves to crystalline silicon as the absorber material, like PERC, TOPCon, HJT, IBC or its variants. For the best performance, the cell should be optimised to harvest the long wavelength photons transmitted by the top cell and feature very well-passivated surfaces. Parasitic absorption in the short wavelength of the solar spectrum is, however, less relevant, since those photons have already been absorbed in the top cell. With the photocurrent being about half of a single-junction silicon cell, the tandem cell is more tolerant to high series resistance, but low-light-intensity performance becomes even more relevant.

Finally, the front side should be textured, as it is with single-junction crystalline silicon. The light

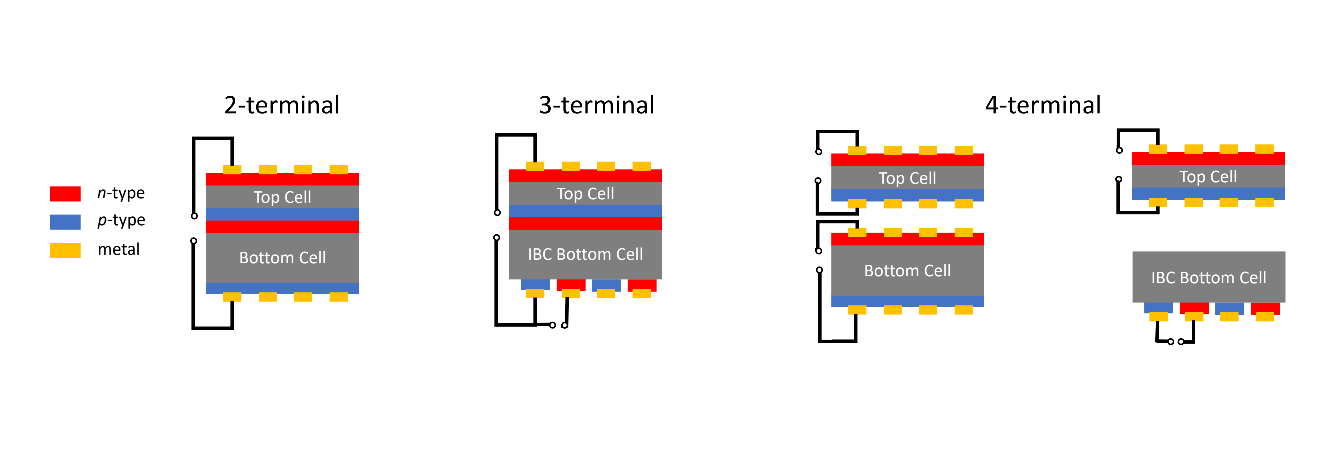


Figure 2: Sketch of tandem cells with two, three or four external contacts. Notably, a 2-terminal configuration requires current matching between both sub cells for optimum performance, while 3- and 4-terminal devices are only optically coupled yet more complex in terms of PV module assembly and maximum power point tracking.

is coupled in effectively and the photons have a longer path length within the tandem cell. A texture on the rear additionally supports the light trapping but is only mandatory when the front side is planarised. Also, a texture on the front side significantly improves the annual energy yield in fixed-tilt installations [3]. However, it is more challenging from a technological point of view to achieve conformal thin film deposition on a textured surface. This imposes technical constraints for the choice of deposition methods, as discussed in more detail later.

Regarding the choice of the best bottom cell, many factors need to be considered. From a commercial perspective, using a standard PERC cell as a bottom cell would likely be the fastest way to achieve large-scale adoption of the tandem concept. However, the integration of a very low-temperature processing route for a perovskite top cell into an overall attractive process flow might prove more complex than initially envisioned. This is because PERC cell manufacturing has been optimised for high-temperature metallisation and fire-through of metal pastes through electrically insulating layers, whereas for a 2-terminal tandem cell, the sub cells also need to be electrically connected to each other through conductive layers. Hence, a full-area passivating front contact of the silicon cell that enables vertical carrier flow, like TOPCon or POLO, can offer a performance benefit [4,5]. The surface passivation is superior to PERC cells yet conductive, which enables the interconnection of the sub cells without patterning process steps. For interconnection to the top cell also a polycrystalline tunnel junction can be employed [10]. While the highly doped poly-silicon layers are rather absorptive in the short wavelength spectrum, this does not compromise the efficiency in a tandem cell because the short wavelength photons are already absorbed in the top cell. However, the established technology for this intermediate interconnection layer is still a recombination TCO.

IBC cells are also amongst potential device structures for perovskite-silicon tandem solar cells. Since an IBC cell has the contacts for the two polarities already on its rear side, a 3-terminal device can be built. Because of the additional third terminal, the requirement for current matching of the two sub cells is lifted. However, for a PV module, the interconnection of the cells in a full-size module is complex when exploiting the third terminal and the practical impact on energy yield depends on the actual circumstances [7].

While a TCO layer may also be applied onto the front side of an IBC, PERC or TOPCon cell [8], an HJT bottom cell naturally already ends with a TCO layer on the front. Moreover, process technologies for HJT and perovskite cells are often very similar (e.g. vacuum equipment). Hence, HJT bottom cells are especially prominent in 2-terminal perovskite-silicon tandem cell development. Also, an HJT cell´s major weak point is often the relatively strong parasitic absorption of short wavelength photons – in a tandem cell, these high energy photons are already absorbed in the top cell, hence this disadvantage becomes unimportant. In combination with a rather simple process flow for a lab environment, these factors have led to HJT becoming the workhorse for 2-terminal perovskite-silicon tandem solar cells, at least in R&D.

When factoring in manufacturing costs and yield in high-volume manufacturing, this might change, and further development efforts will continue with many variants of silicon solar cell device structures as the bottom cell.

While all discussed bottom cell types are already in PV mass manufacturing, this is not yet the case for all layers of the top cell. The function and examples of the individual layers are discussed in more detail in the following.

Interconnection layer

In monolithic series connected tandem solar cells, the interconnection layer electrically connects the sub cells. Ideally, this is done without voltage losses at the transition between the sub cells and without parasitic absorption in the interconnection layer for infrared light, which should be absorbed in the silicon bottom cell.

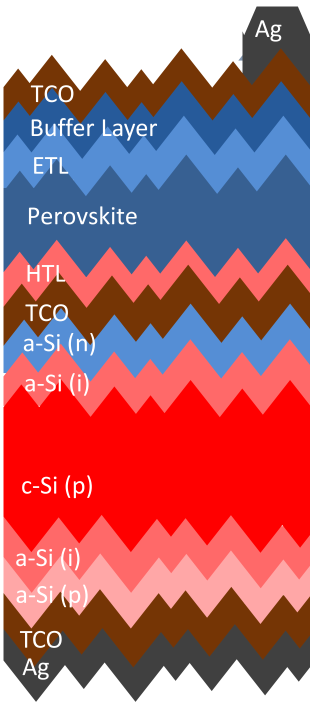
Such an interlayer prevents the formation of a blocking pn-junction between the hole contact of the top cell and the electron contact of the silicon cell. Conventionally, either a recombination layer or a tunnel junction are used. Tunnel junctions are widely and very successfully used in III-V multijunction cells [9]. The tunnel junction itself is made by one degenerately doped n++ layer and one p++ layer, and the carrier transport takes place as tunnel current above the very narrow depletion layer. Such a tunnel diode can be realised, e.g., by PECVD deposited and annealed poly-Si layers, as shown by Luderer et al. [10].

Alternatively, so-called recombination layers can be used. These layers act like a conductive layer, which can transport electrons and holes. So, the electrons from the silicon cell recombine with the holes from the top cell. The simplest example is evaporated ultra-thin metal films, which are used, e.g., in organic-based tandem cells [11]. These metal layers have to be thin enough to avoid parasitic absorption. An often-used recombination layer in a Pero-Si Tandem solar cell is ITO or other metal oxide layers [12], which can be easily deposited by sputtering. ITO is a good conductor for electrons and holes, which is why it is used for both polarities in silicon heterojunction solar cells. The thickness of the metal oxide layer should also be thin enough, not only for low absorption, but also to avoid optical interference effects, leading to unwanted reflections.

Several different options for industrial depositions of the interconnection layer are available, and the choice largely depends on the overall device design and process integration.

Hole Transport Layer (HTL)

Depending on the deposition sequence, the top cell configuration is either a n-i-p or p-i-n structure. First reports on pero-si tandem devices were built in the n-i-p layer sequence but poor optics caused by a thick layer of the hole transport material Spiro-OMeTAD limited device performance. Since 2017 most publications focus on the inverse p-i-n structure, where the hole transport layer (p-type) is deposited first. In the following we focus on this particular structure, however, it is noteworthy that the choice of



Buffer Layer, e.g. SnO, Al_2O_3, etc.

ETL: Electron Transport Layer C60

HTL: Hole Transport Layer, e.g. NiO, SAM, etc.

TCO: Transparent Conductive Oxide e.g. ITO, AZO, IZO, etc.

Figure 3: Sketch of a textured perovskite-silicon tandem solar cell with a p-type HJT bottom cell, as used for development at Fraunhofer ISE. There are several options for the choice of materials and their deposition methods, and these are being continuously investigated in the PV community.

p-i-n vs n-i-p depends on the development of suitable charge transport materials. Common examples for suitable hole transport layers in the p-i-n structure are wet chemically applied self-assembling monolayers (SAM) such as 2PACz and Me-4PACz [13,14].

Moreover, vacuum-based processes are suited for conformal coating on textured surfaces. Thin evaporated Spiro-TTB [15] has been reported, however, they show film degradation in the form of melting into the valleys (due to low glass transition temperature) upon temperature treatment above 150°C [17]. Such temperature is commonly used for thermal annealing of the perovskite layer on texture as well as curing of metal paste. As an alternative, sputtered NiOx can be deployed, most likely in combination with a subsequent deposition of SAMs [16] (for improved stability and minimized surface recombination).

Evaporation of organic compounds or sputtering of metal oxides are methods that can be adopted to the requirements of wafer-based high-volume manufacturing.

Perovskite

The deposition of the perovskite absorber on a large wafer area can be accomplished by several methods. Spin-coating is a very versatile technology, but it is restricted to small areas and only utilises a small fraction of the prepared chemical solution. Slot-die coating is not only used on perovskite single-junction thin-film modules but can also be used for silicon-based perovskite-silicon tandem solar cells [18]. However, when applied on textured silicon, the texture is basically filled up and the perovskite surface is mostly planarised [19].

Two methods for a conformal coating of textured silicon that preserve the texture are co-evaporation [20,21] and the hybrid route combining co-evaporation and wet chemical processing [22]. They have shown very promising results that are likely to be scalable to a large wafer area and also could be envisioned to be manufacturable on an industrial scale [23].

In the hybrid route, the deposition of the perovskite is split into two process steps.

In the first step, the inorganic components are thermally evaporated to form a scaffold, allowing the conformal coating of pyramids of arbitrary size and shape. In the second step, the conversion into perovskite is accomplished by infiltration with organic salt solutions. For the second step, several deposition techniques have been evaluated by researchers and are already used in industrial fields like spray coating, inkjet printing and slot-die coating (see Figure 4).

The benefit of this approach is that a conformal coating of the pyramids can be achieved and the texture is preserved.

Thermal annealing at temperatures around 130–150°C completes the conversion process and the formation of perovskite. The difficulty with this hybrid process flow is to ensure a good infiltration of the organics into the scaffold and complete conversion into a high-quality perovskite crystal without remnant PbI_2 at the lower interface. Alternatively, the entire perovskite can be evaporated in a single process step [21,22] (co-evaporation of inorganic and organic components). Alternatively, it can even be achieved sequentially, where the inorganic layer is deposited first and an organic layer is subsequently deposited on top [24]. Such two-step processing minimises the use of expensive and potentially harmful solvents in the process flow and separates the evaporation of the organic materials from the inorganic ones, which may be a significant advantage from an equipment and process stability point of view.

Electron Transport Layer (ETL)

For efficient current collection, an ETL must be deposited. C60 can be evaporated and serves the purpose reasonably well. However, parasitic absorption is high and the interface is not well passivated, leading to significant losses in all solar cell parameters. To improve this interface, an additional layer can be introduced between the perovskite and the C60. LiF has been shown to improve the passivation by a field effect [25], but the stability of the cells is severely compromised. Recently, Liu et al. [26] proposed MgF_2 as an alternative, with good results and strongly improved stability. It appears that it is less important which layer exactly is deposited, so long as there is a thin layer between the perovskite and the C60 in order to prevent direct contact between the two, similar to the concept of contact displacement in the metal–silicon contact of high-efficiency silicon solar cells [27].

C60 is evaporated and this is, in principle, a scalable process for mass manufacturing. Despite its shortcomings with respect to absorption and recombination, it still appears to currently be the state-of-the-art material for the ETL.

Transparent Conductive Oxide (TCO)

Because of the extremely low conductivity of the bulk perovskite, lateral electrical transport is hampered and a conductive, yet transparent, layer must be placed on top. ITO is the most prominent candidate due to its track record in HJT cell technology. However, cost considerations and limited availability present strong drivers towards the choice of alternatives like AZO or bi-layers [28]. Fortunately, developments from HJT technology aim in the same direction of improving transparency and conductivity. Furthermore, sputtering technology to deposit TCOs is already established for solar cell production in high-volume manufacturing.

Buffer layer

Sputtering of a TCO can result in significant sputtering damage to the ETL. To avoid or at least reduce the damage, a thin buffer layer may be placed between the C60 and the TCO, like SnOx [29]. Such thin layers may be deposited by ALD, which has been used for the deposition of Al2O3 in industrial PERC processing.

Metallisation

In lab environments where the test cells are small (of the order of square centimetres), usually narrow traces of thin silver are evaporated as a front electrode. Alternatively, and suitable for an industrial process, screen-printing of ultra-low temperature silver paste can be employed. The

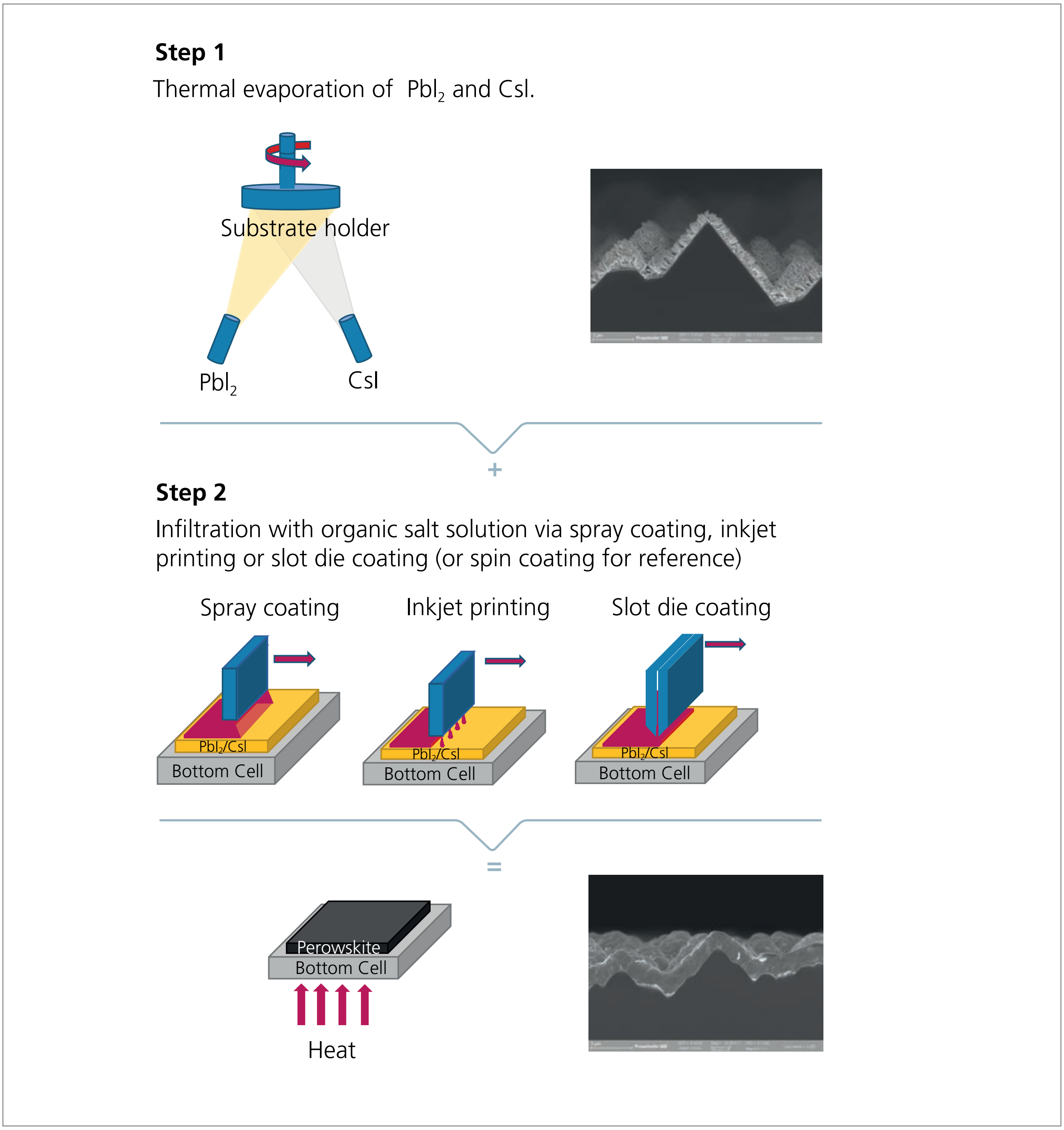


Figure 4: Hybrid process route for conformal coverage of a textured silicon bottom cell. Step 1: Deposition of a thin film of the inorganic components (e.g. CsI, PbI2, CsBr or PbBr2). Step 2: Exposure of the inorganic thin film to the organic component from solution. After subsequent thermal annealing the precursors are converted to the perovskite thin film. The thin film is converted to perovskite.

paste must adhere to the surface and provide good electrical contact and line resistance, even though the curing temperature is limited to about 150°C to prevent damage to the perovskite top cell with all its layers. This low-temperature requirement puts severe constraints on the paste composition and printability; it even exceeds the requirement of HJT cells. Screen-printing of silver paste is the standard method for the metallisation process in the PV industry. It has successfully been applied on perovskite-silicon tandem solar cells [30,31] and upscaling to larger areas has also successfully been demonstrated [23].

Anti-reflection coating

The standard process for the anti-reflection coating on single-junction crystalline silicon solar cells consists of a silicon nitride film with a refractive index of about n_{SiNx}~2 by PECVD. This is in between the refractive indices of the encapsulant/glass of n_{glass}~1.5 on the front side and the silicon wafer $n_{silicon}$~4, and effectively improves incoupling of sunlight. In a perovskite-silicon tandem cell, however, the refractive index of the perovskite is much lower than silicon $n_{perovskite}$~2.5 and there is no need to add an ARC for perovskite-silicon tandem solar cells for use in encapsulated PV modules [32].

Whether a more efficient PV module results in a lower cost of electricity depends on, besides other factors, whether the additional efficiency is obtained in a cost-effective way. In the following cost calculations, we shed light onto the relationship of cost and efficiency increase based on certain assumptions.

Cost calculations

As mentioned before, for large-scale implementation of perovskite-silicon tandem solar cells, viable bottom cell candidates are PERC, TOPCon, SHJ and IBC. Wu et al. [4], e.g., published results for a device based on an industrial TOPCon bottom cell process route, achieving 27.6%.

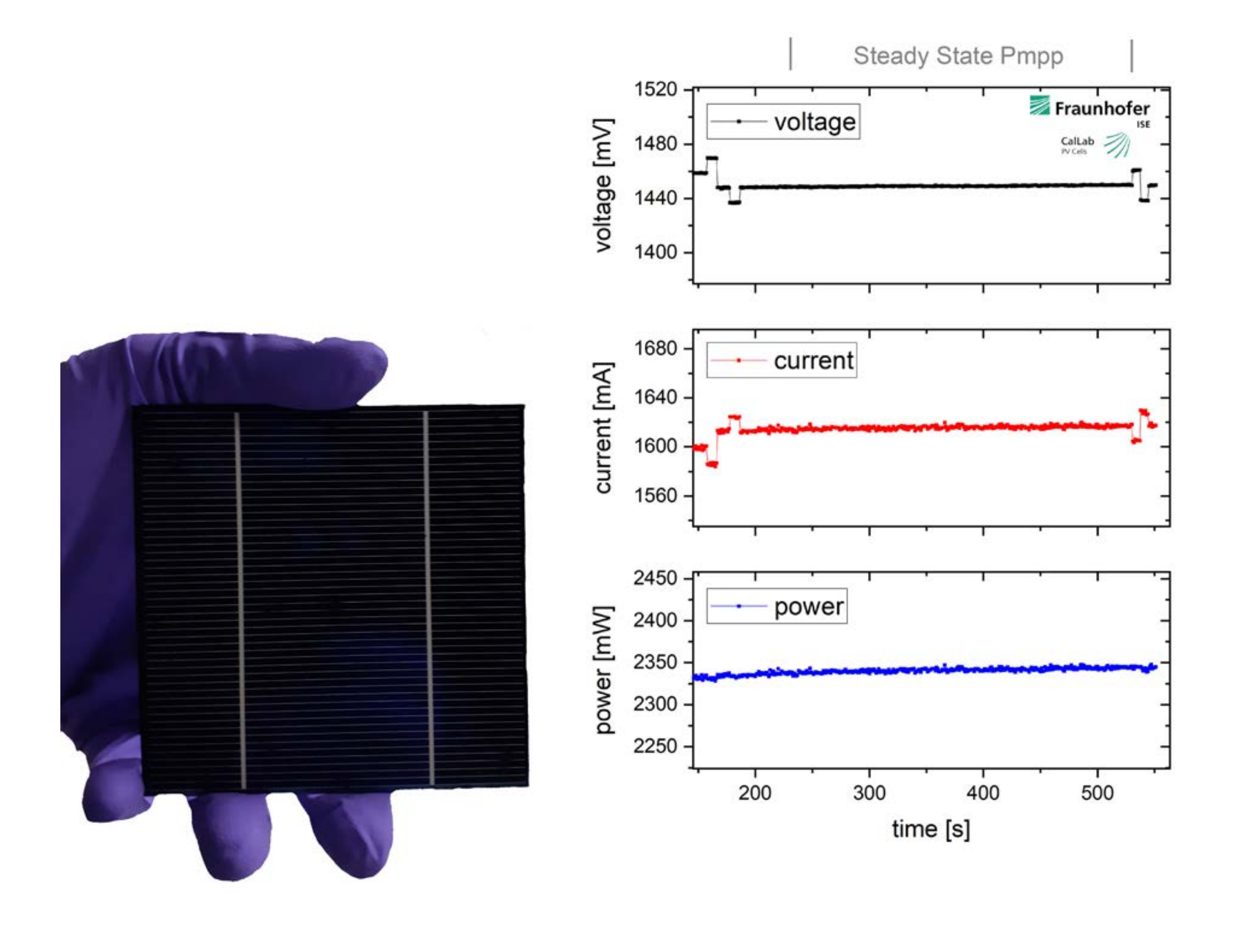


Figure 5: 104 cm² perovskite-silicon tandem solar cell with screen-printed front metallisation fabricated at Fraunhofer ISE. Power conversion efficiency of 22.5% under steady-state measurement conditions certified by Fraunhofer ISE CalLab Cells.

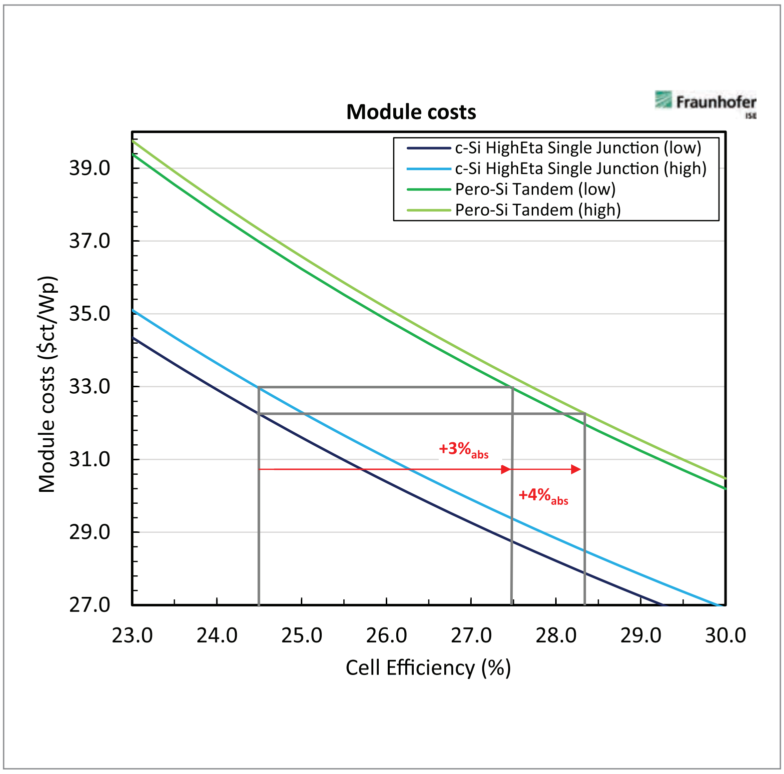


Figure 6: Impact of the cell device efficiency on the module cost for the total cost of ownership calculation. For a cell efficiency of 24.5% for single-junction devices, an efficiency advantage of 3–4%$_{abs.}$ is required for the tandem cells to reach the same module costs. The terms "low" and "high" refer to the low-cost or high-cost options, respectively, within the investigated device structures and process flows.

Messmer et al. [33] compared PERC, TOPCon and SHJ to potentially serve as silicon bottom cell devices, based on device simulations and a bottom-up total cost of ownership assessment. Updated cost calculations at Fraunhofer ISE, using M10 TOPCon or HJT as bottom cells, show that with a PVD-based hybrid route for the processing of the perovskite top cell, the required CAPEX investment for tandem cell production equipment increases by 40–90% over a single-junction counterpart for a 10 GWp factory. The operational costs (OPEX) for the tandem cell production (without depreciation and costs for the silicon wafer) increase by 50–90%. However, the high levels of uncertainty regarding economies of scale for the current low-volume perovskite top cell materials significantly impact the OPEX of the top cell device.

Assuming an M10 silicon n-type wafer price of 1 USD per piece currently (December 2022), a cell efficiency advantage of 3–4%abs. for the tandem cells would be required to reach a similar full cell cost per Wp to the standalone c-Si single-junction devices.

Integrating the tandem cells into a module requires additional encapsulation measures to be taken into account for assuring device stability. Assuming these measures correspond to additional module production costs (without the cells) of about 20%, with the same cell-to-module loss/gain, the full module production costs for the tandems would reach the same level per Wp as the c-Si single-junction modules. Thus, our total cost of ownership calculations show that a module efficiency advantage of 3–4%abs. for the tandem devices leads to similar production costs per Wp for the module level as for the c-Si single-junction technologies (see Figure 6).

The tandem-related efficiency benefit transfers further to the costs downstream of the PV-system level, since with the same PV-system area and balance-of-system (BOS) related costs, more system capacity can be installed. In the end, the levelised cost of electricity (LCOE) will remain the final measure of the viability of a new cell technology.

Conclusion

Monolithic perovskite-silicon tandem solar cells offer an attractive option for further efficiency increases in photovoltaic modules. The device design and process flow are still under intense development. Several potential solutions have emerged and are promising candidates for successful product development on a commercial scale. While the production equipment for perovskite solar cells is different from traditional crystalline silicon cells, some processes like evaporation or sputtering can already be found in the thin-film PV segment or in HJT production lines. Hence, part of the upscaling effort might be accomplished by modification of existing tools. For a successful launch of perovskite-silicon tandem solar cells, the efficiency increase at moderate cost will need to be proven on a full wafer area and on production tools capable of high-volume manufacturing. The perovskite-silicon tandem cells will have to demonstrate bankability and stability in the field for successful commercialisation. With the progress achieved to date and the current investment for R&D from the public sector as well as from industry, it should only be a matter of time before PV modules make the next major efficiency leap forward.

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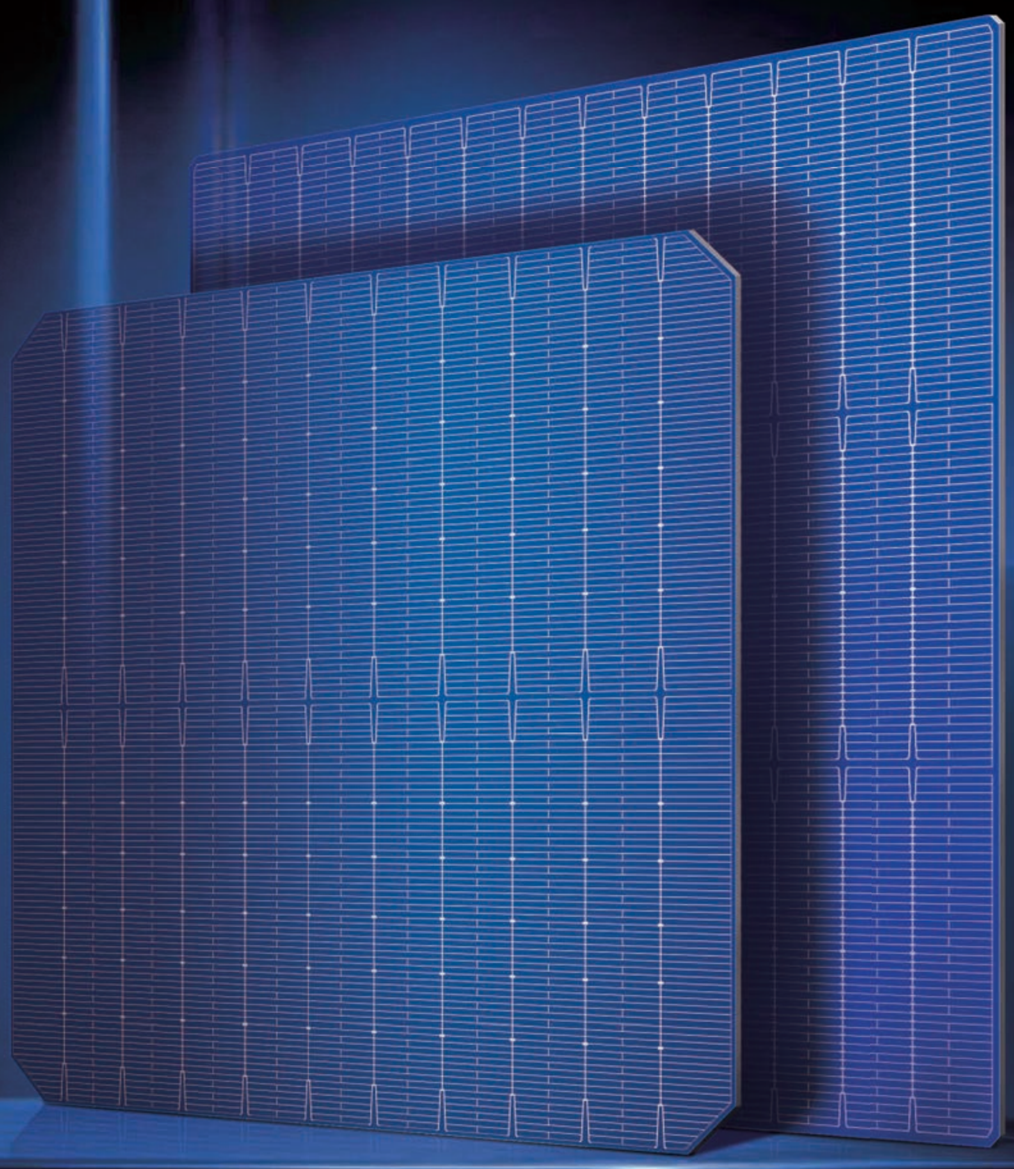

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